OD5160

T-CON product brief

New TED IC (T-CON Embedded Driver IC) with More Cost Advantage, Lower Power Consumption for Next-Generation Notebook Displays

OMNIVISION Display Solutions' OD5160 TED IC leverages OMNIVISION's proven image algorithms, slim bezel topology, power saving technology, powerful driving design, high quality and stable supply chain to help tier-one notebook panel manufactures provide all-in-one total display solution and speed time to market.

OD5160 can provide 1-chip solutions for 2160 x 1350 (LTPS), 1920 x 1080/1200/1280 (a-Si, Oxide, and LTPS) LCD TFT panels to make low cost and low power consumption. OD5160 can support 2880ch source driver output, 2-lane eDP with HBR, R243, R216, and RBR input interface.

OD5160 can provide 1-chip solutions for dual gate panels and 2-chip solutions with VESA MSO (multi-SST operation) feature. In case of 2-chip solutions, OD5160 can support up to 2880 x 1920 resolution.

OD5160 integrates level shifter to directly drive panel GIP, and it can support up to 42ch. It also supports an external I2C and SPI interface for EEPROM and PMIC. System development kits (SDK) are available to enable fine-tuning and optimization panel characteristics. Meanwhile, OD5160's chip size and bump position are pin compatible with CRX2000A.

Find out more at www.ovt.com.

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OD5160

Ordering Information

- **OD5160-A0S-EGV40Z-0** (general customers, 4 inch tray)
- **OD5160-A0S-EGV30Z-0** (general customers, 3 inch tray)

Applications

- notebooks

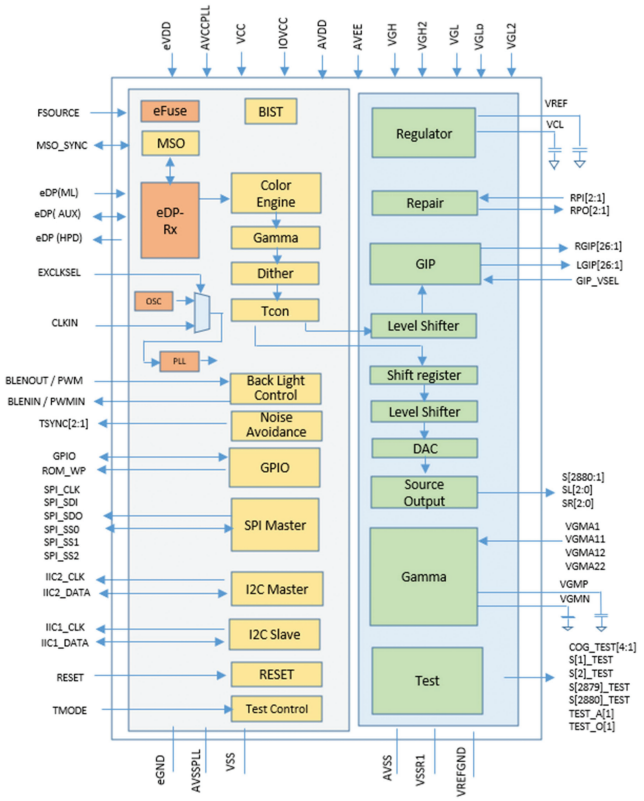
General Features

- **common features:**
  - power supply
    - logic supply voltage: 1.2V
    - LCD driving voltage: AVDD 4.0V ~ 6.0V, AVEE -6.0V ~ -4.0V
    - IOVCC 3.0V ~ 3.6V
    - output dynamic range: -5.8V (>AVEE+0.2V) to GNDA-0.2, GNDA+0.2 to 5.8V (<AVDD-0.2V)
    - VGH supply voltage +8V ~ +20V
    - VGL, VGLp supply voltage -7V ~ -15V
    - VGH-VGL must be less than 32V
  - COG package
  - operation temperature: -20°C ~ +85°C
  - butterfly fanout wiring for narrow bezel solution
- **eDP features:**
  - HBR (2.7 Gbps), R243 (2.43 Gbps), R216 (2.16 Gbps), RBR (1.62 Gbps)
  - 1 and 2 lanes main link configuration
  - MSO (multi-SST operation)
  - high noise tolerant eDP PHY working on COG
  - AdaptiveSync, FreeSync, SDRRS (real performance depending on panel loading and system configuration)
  - I2C-over-aux
  - SSC 0.5% down-spreading

General Features (continued)

- **T-CON features:**
  - programmable GIP signals up to 42 outputs for GIP panel (left x21, right x21)
  - SDK (system development kit to light-up, debug and fine-tune easily)
  - APPS (advanced panel power saving) low power architecture
  - I2C and SPI serial port interface master/slave
  - 18/24-bit RGB input
  - digital gamma
  - color management
  - noise avoidance for touch panel
  - panel BIST mode
  - support CABC
  - pattern detection
- **GIP features:**
  - programmable GIP signals up to 42 outputs for GIP (left x21, right x21)
  - HV output mode and 3.3V (IOVCC) output mode
  - integrated level shifter
  - support single gate, dual gate driving method
  - EQ function of GIP output
- **source driver features:**
  - 2886/2880/2166/2160/1926/1920 output channels
    - 2160 x 1350, 1920 x 1280, 1920 x 1200, 1920 x 1080 for 1-chip solutions
    - up to 2880 x 1920 for 2-chip solutions
  - 8-bit resolution / 256 gray scale
  - N-dot (N=1/2) and N-line (N=1/2/4) inversion display function provided
  - repair amplifier
  - embedded gamma buffers
  - adjusting gamma correction
  - low frame rate for saving power consumption
  - contact resistance measurement
  - multi zones polarity
  - multi zones skew
  - cool charging to drive heavy RC loading
  - register control function
    - output channel select function
    - line-repair amp enable
    - programmable gamma function
    - source output chopper control
    - gamma output chopper control
    - source driving control for power saving

Functional Block Diagram



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