WL2864C

7-Channel LDO PMIC for Camera Applications

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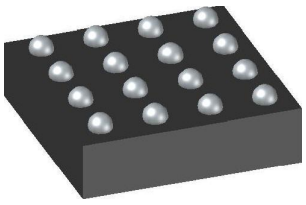
Descriptions

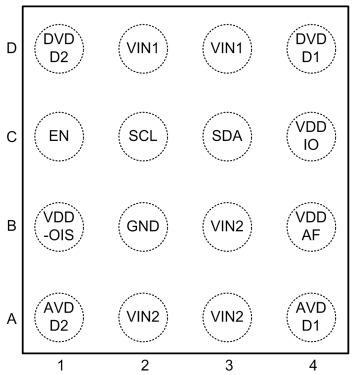
The WL2864C is a 7-Ch integrated LDOs for camera sensor applications include 2-Ch DVDD, 2-Ch AVDD, 1-Ch VDDIO, 1-Ch VDDAF, 1-Ch VDDOIS. With 400KHz high speed I2C interface, the function setting is flexible such as power sequence, output voltage, output discharge, current limit per channel. The chip enable control support EN pin control and I2C control.

Due to high load current and lower working voltage of DVDD, WL2864C used N-MOSFET LDO architecture without charge pump for 2-Ch DVDD LDO. DVDD LDO input source is VIN1 and VIN2 is the bias voltage. Ultra low dropout voltage (Typ. 75mV @ 0.5A Load) of DVDD LDOs is designed for high efficiency and lower power dissipation purpose. For other 5-Ch LDOs (AVDD, VDDIO, VDDAF, VDDOIS), WL2864C used P-MOSFET LDO architecture. The input source is VIN2. Due to high performance requirement of AVDD, WL2864C's AVDD used special circuit design and optimized pin assignment which is easy for system PCB layout.

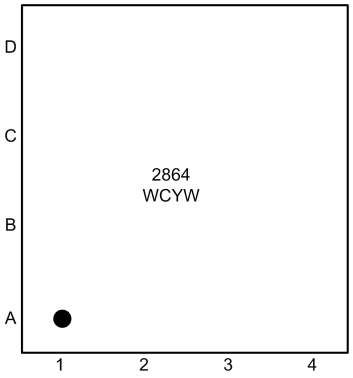
Highly integrated, small package size is also very suitable for smart phone applications. WL2864C is available in 1.6x1.6mm 16 ball wafer level chip scale package. Standard products are Pb-free and halogen-free.



CSP-16L (Bottom View)



Pin Configuration (Top View)



Marking

2864 : Device Code
WC : Special Code
Y : Year Code (A~z)
W : Week Code (A~z)

Features:

- VIN1 input voltage range : 0.6V~2.0V
- LDO1/2 output voltage range : 0.6V~1.8V
- LDO1/2 dropout voltage : 75mV@0.5A
- LDO1/2 output current : 600mA Max.
- VIN2 input voltage range : 3.0V~5.5V
- Other LDO output voltage range : 1.2V~4.3V
- Other LDO dropout voltage : See EC table
- Other LDO output current : See EC table
- AVDD LDO PSRR : 92dB
- AVDD LDO output noise : 15uV

Order Information

Device	Package	Shipping
WL2864C-16/TR	CSP-16L	3000/Reel&Tape

Applications:

- Smart Phone
- IP Camera
- Camera Module

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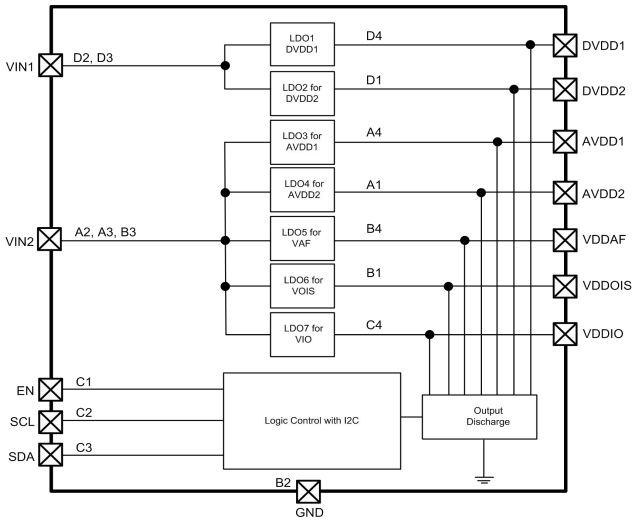
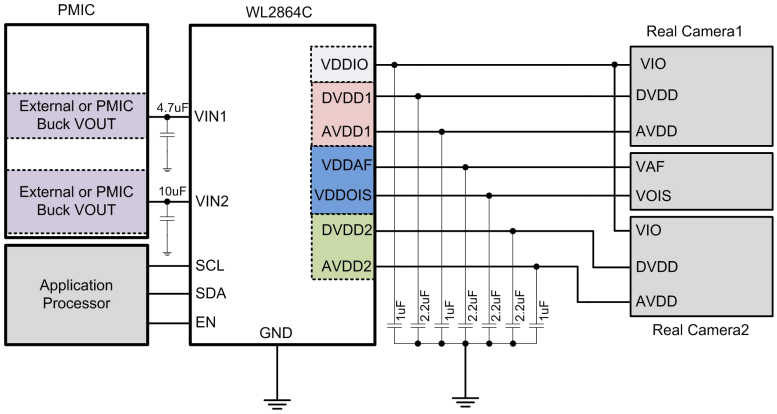
Block Diagram



PIN Descriptions

Pin No.	Symbol	Description
D2, D3	VIN1	LDO1, LDO2 supply input
D1	DVDD2	LDO2 regulate output
D4	DVDD1	LDO1 regulate output
A2, A3, B3	VIN2	LDO3~LDO7 Supply input, LDO1, LDO2 bias
A1	AVDD2	LDO4 regulator output
A4	AVDD1	LDO3 regulator output
B4	VDDAF	LDO5 regulator output
B1	VDDOIS	LDO6 regulator output
C4	VDDIO	LDO7 regulator output
B2	GND	Ground
C1	EN	Global enable control, Active high. Maintain to low if I2C control used
C2	SCL	I2C interface
C3	SDA	

Typical Applications



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Absolute Maximum Ratings

Parameter		Value	Unit
V_{IN} Range (VIN1 ,VIN2)		-0.3~6.5	V
V_{EN} Range		−0.3 to V_{IN} + 0.3	V
V_{OUT} Range		−0.3 to V_{IN} + 0.3	V
I_{OUT}		Check EC table	mA
Lead Temperature Range		260	°C
Storage Temperature Range		-55 ~ 150	°C
Operating Junction Temperature Range		150	°C
ESD Ratings	HBM	7000	V
	MM	300	V

These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Recommend Operating Ratings

Parameter	Value	Unit
VIN1 Operating Supply Voltage Range	0.6~2.0	V
VIN2 Operating Supply Voltage Range	3.0~5.5	V
Operating Temperature Range	-40～85	°C
Thermal Resistance, $R_{\theta JA}$ (note)	188	°C/W

Note:

Surface mounted on FR4 Board using 1.5*1.5 inch^2 FR4 , copper(1 inch^2/1 Oz)

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Electronics Characteristics (V_{IN}=V_{OUT}+1V, C_{IN}=C_{OUT}=1uF, Ta = +25°C, unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Whole Device						
Quiescent current at all LDO active	I_Q	EN=H or Enable chip by I2C, No load		100	130	uA
Shutdown current	I_{SHDN}	EN=L or Shutdown by I2C			1	uA
EN logic high voltage	V_{ENH}		1.2			V
EN logic low voltage	V_{ENL}				0.4	V
EN pin leakage current	I_{EN}	VEN= 0 to 5.5V			1	uA
Turn−On Time	T_{ON}	EN=L to H, V_{OUT}=1.2V LDO1/2 V_{OUT}=V_{OUT} * 90%		0.8		mS
		EN=L to H, V_{OUT}=2.8V, LDO3~6 V_{OUT}=V_{OUT} * 90%		0.8		mS
		EN=L to H, V_{OUT}=1.8V LDO7 V_{OUT}=V_{OUT} * 90%		0.6		mS
Thermal shutdown threshold	T_{SDH}	Iout=1mA		150		ºC
Thermal shutdown hysteresis	$T_{SDH-HYS}$	Iout=1mA		25		ºC
Output discharge resistor ON resistance	R_{DCHG}	EN=L or Shutdown by I2C		350		Ω
Under voltage lock-out	$UVLO_{\_VIN1}$	VIN1 Falling		N.A		V
	$UVLO_{\_VIN2}$	VIN2 Falling		1.9		V
ULVO hysteresis	$UVLO_{\_HYS}$	VIN Rising		0.1		V

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Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LDO1, LDO2 (DVDDx)						
Input voltage range	VIN1		0.6		2.0	V
Output voltage range	DVDDx		0.6		1.8	V
Default output voltage	DVDDx	EN=H		1.2		V
Output voltage accuracy	V_{OUT_ACC}		-2		+2	%
Output current limit	I_{LIM}	RL=1Ω	600			mA
Short current	I_{SHORT}	V_{OUT}=GND		900		mA
Dropout voltage	V_{DROP}	VIN2=3.0V, V_{OUT}=1.05V, I_{OUT}=500mA		75		mV
		VIN2=3.0V, V_{OUT}=1.2V, I_{OUT}=500mA		90		mV
	V_{DROP}	VIN2=3.3V, V_{OUT}=1.05V, I_{OUT}=500mA		62		mV
		VIN2=3.3V, V_{OUT}=1.2V, I_{OUT}=500mA		68		mV
Load regulation	$\triangle V_{Load}$	VIN2=3.3V, VIN1=1.3V, V_{OUT}=1.2V, I_{OUT}=1~200mA		12		mV
Line regulation	$\triangle V_{LINE}$	VIN2=3.3V, VIN1=1.25~2.0V V_{OUT}=1.2V, IOUT=10mA		0.1		mV
		VIN2=3.0～4.0V, VIN1=1.3V V_{OUT}=1.2V, IOUT=10mA		0.5		mV
Output voltage noise	e_{NO}	VIN2=3.3V, VIN1=1.3V V_{OUT}=1.2V, 10Hz to 100KHz		50		uV
Power Supply Rejection Rate	$PSRR_{\_VIN1}$	VIN1=1.6V+0.2V_{P-P} VIN2=3.8V, V_{OUT}=1.05V I_{OUT}=10mA, F=1KHz, C_{OUT}=2.2uF		43		dB
	$PSRR_{\_VIN2}$	VIN2=3.8V+0.2V_{P-P} VIN1=1.6V, V_{OUT}=1.05V I_{OUT}=10mA, F=1KHz, C_{OUT}=2.2uF		36		dB

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Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LDO3, LDO4 (AVDDx)						
Input voltage range	VIN2		3.0		5.5	V
Output voltage range	AVDDx		1.2		4.3	V
Default output voltage	AVDDx	EN=H		2.8		V
Output voltage accuracy	V_{OUT_ACC}		-2		+2	%
Output current limit	I_{LIM}	RL=1Ω	350			mA
Short current	I_{SHORT}	V_{OUT}=GND		500		mA
Dropout voltage	V_{DROP}	V_{OUT}=2.8V, I_{OUT}=300mA		95		mV
Load regulation	$\triangle V_{Load}$	VIN2=3.3V, V_{OUT}=2.8V, I_{OUT}=1~200mA		10		mV
Line regulation	$\triangle V_{LINE}$	VIN2=3.0V~4.0V, V_{OUT}=2.8V, IOUT=10mA,		0.2	1	mV
Output voltage noise	e_{NO}	VIN2=3.3V, V_{OUT}=2.8V, 10Hz to 100KHz		8		uV
Power Supply Rejection Rate	PSRR	VIN2=3.8V+0.2V_{P-P} V_{OUT}=2.8V, I_{OUT}=10mA, F=1KHz, C_{OUT}=1uF		92		dB
		VIN2=3.8V+0.2V_{P-P} V_{OUT}=2.8V, I_{OUT}=100mA, F=1KHz, C_{OUT}=1uF		90		dB
		VIN2=3.8V+0.2V_{P-P} V_{OUT}=2.8V, I_{OUT}=10mA, F=1MHz, C_{OUT}=1uF		30		dB
		VIN2=3.8V+0.2V_{P-P} V_{OUT}=2.8V, I_{OUT}=100mA, F=1MHz, C_{OUT}=1uF		37		dB
		VIN2=3.8V+0.2V_{P-P} V_{OUT}=2.8V, I_{OUT}=10mA, F=1MHz, C_{OUT}=22uF		67		dB
		VIN2=3.8V+0.2V_{P-P} V_{OUT}=2.8V, I_{OUT}=100mA, F=1MHz, C_{OUT}=22uF		67		dB

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Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
LDO5, LDO6 (VDDAF, VDDOIS)						
Input voltage range	VIN2		3.0		5.5	V
Output voltage range	VDDAF/OIS		1.2		4.3	V
Default output voltage	VDDAF/OIS	EN=H		2.8		V
Output voltage accuracy	V_{OUT_ACC}		-2		+2	%
Output current limit	I_{LIM}	RL=1Ω	600			mA
Short current	I_{SHORT}	V_{OUT}=GND		900		mA
Dropout voltage	V_{DROP}	V_{OUT}=2.8V, I_{OUT}=300mA		70		mV
		V_{OUT}=3.3V, I_{OUT}=300mA		60		mV
Load regulation	$\triangle V_{Load}$	VIN2=3.3V, V_{OUT}=2.8V, I_{OUT}=1~200mA		5		mV
Line regulation	$\triangle V_{LINE}$	VIN2=3.0V~4.0V, V_{OUT}=2.8V, IOUT=10mA,		0.1		mV
Output voltage noise	e_{NO}	VIN2=3.3V, V_{OUT}=2.8V, 10Hz to 100KHz		10		uV
Power Supply Rejection Rate	PSRR	VIN2=3.8V+0.2V_{P-P} V_{OUT}=2.8V, I_{OUT}=10mA, F=1KHz, C_{OUT}=2.2uF		88		dB
		VIN2=3.8V+0.2V_{P-P} V_{OUT}=2.8V, I_{OUT}=100mA, F=1KHz, C_{OUT}=2.2uF		90		dB
LDO7 (VDDIO)						
Input voltage range	VIN2		3.0		5.5	V
Output voltage range	VDDIO		1.2		4.3	V
Default output voltage	VDDIO	EN=H		1.8		V
Output voltage accuracy	V_{OUT_ACC}		-2		+2	%
Output current limit	I_{LIM}	RL=1Ω	160			mA
Short current	I_{SHORT}	V_{OUT}=GND		220		mA
Dropout voltage	V_{DROP}	V_{OUT}=2.8V, I_{OUT}=300mA		72		mV
		V_{OUT}=3.3V, I_{OUT}=300mA		65		mV
Load regulation	$\triangle V_{Load}$	VIN2=3.3V, V_{OUT}=2.8V, I_{OUT}=1~200mA		6		mV
Line regulation	$\triangle V_{LINE}$	VIN2=3.0V~4.0V, V_{OUT}=2.8V, IOUT=10mA,		0.1		mV
Output voltage noise	e_{NO}	VIN2=3.3V, V_{OUT}=2.8V, 10Hz to 100KHz		15		uV
Power Supply Rejection Rate	PSRR	VIN2=3.8V+0.2V_{P-P} V_{OUT}=2.8V, I_{OUT}=10mA, F=1KHz, C_{OUT}=1uF		100		dB
		VIN2=3.8V+0.2V_{P-P} V_{OUT}=2.8V, I_{OUT}=100mA, F=1KHz, C_{OUT}=1uF		88		dB

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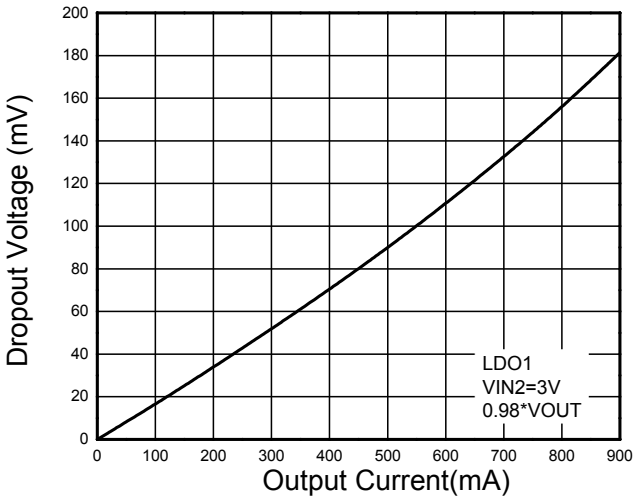
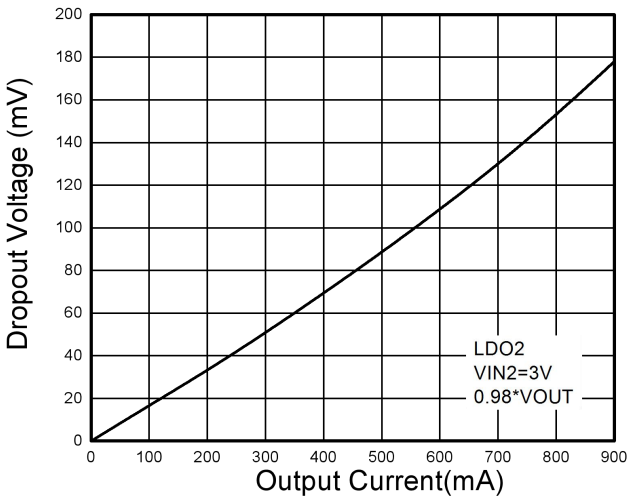
Typical Characteristics (T_A=25°C, unless otherwise noted)

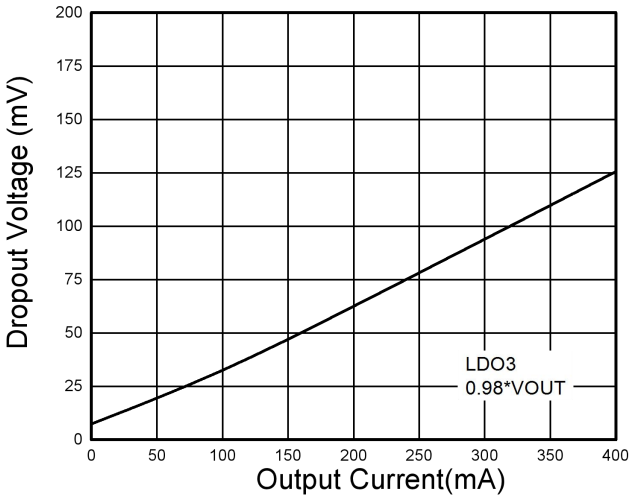
Dropout Voltage



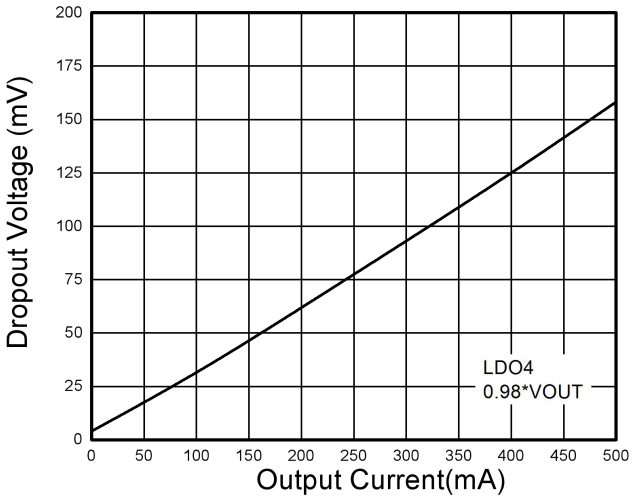
Dropout Voltage vs. Output Voltage



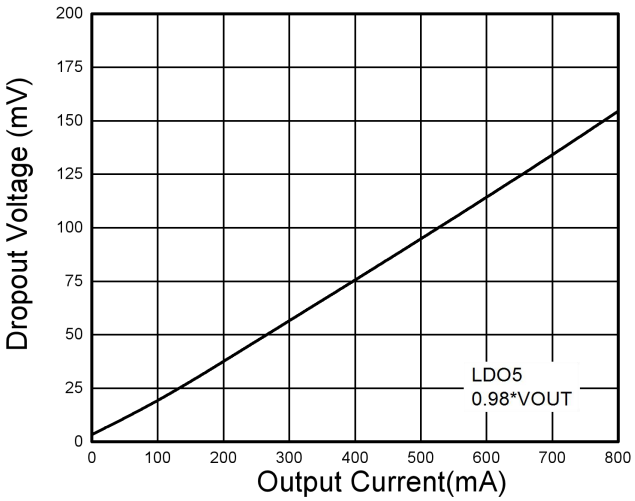
Dropout Voltage vs. Output Voltage



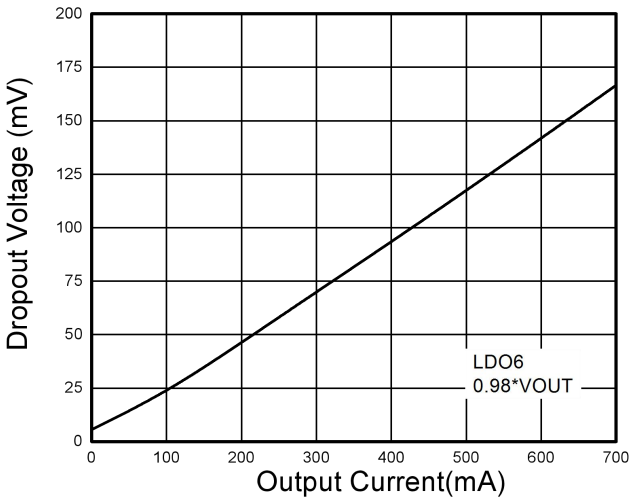
Dropout Voltage vs. Output Voltage



Dropout Voltage vs. Output Voltage



Dropout Voltage vs. Output Voltage



Dropout Voltage vs. Output Voltage

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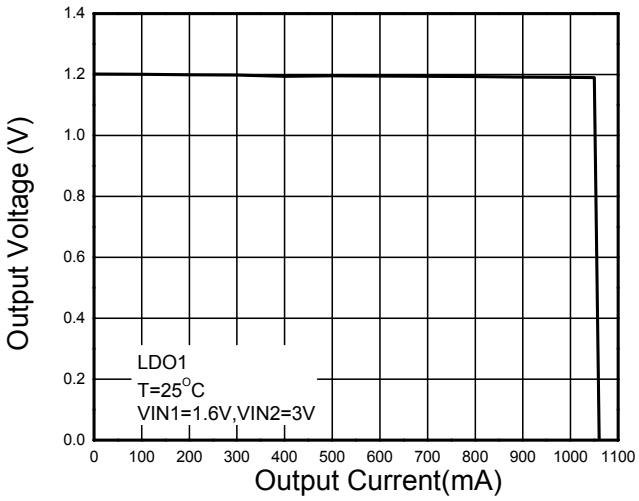
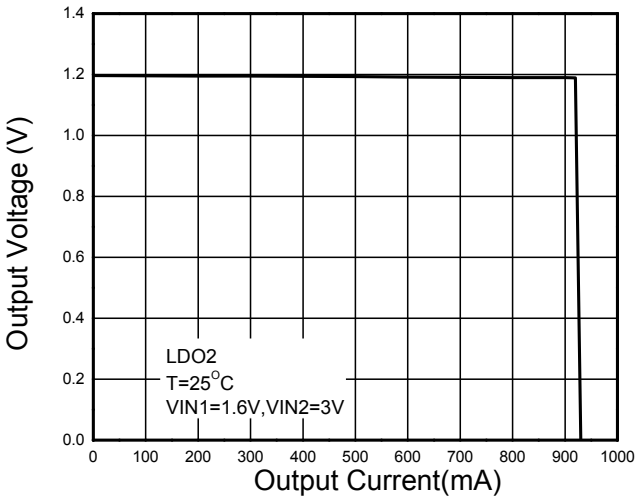
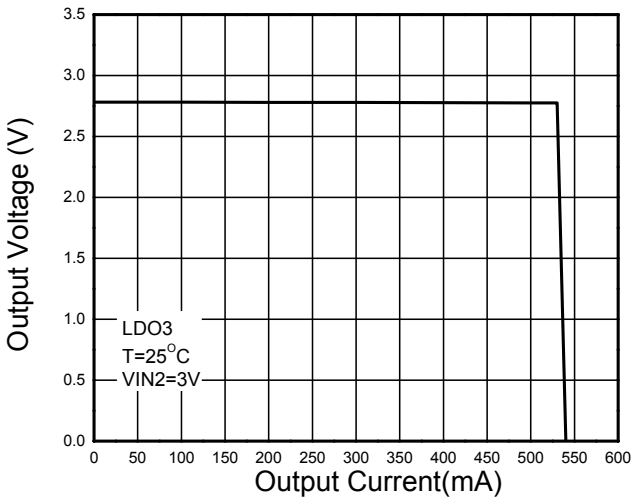
Output Current



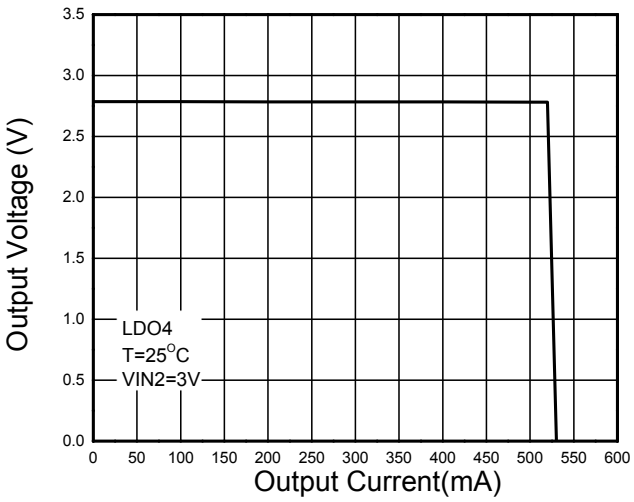
Output Voltage vs. Output Current



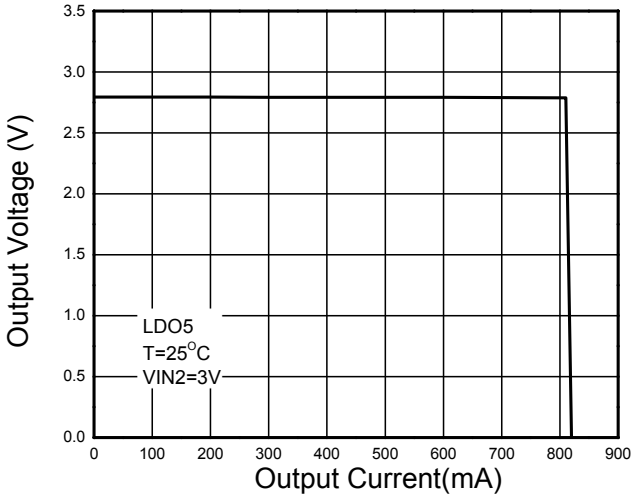
Output Voltage vs. Output Current



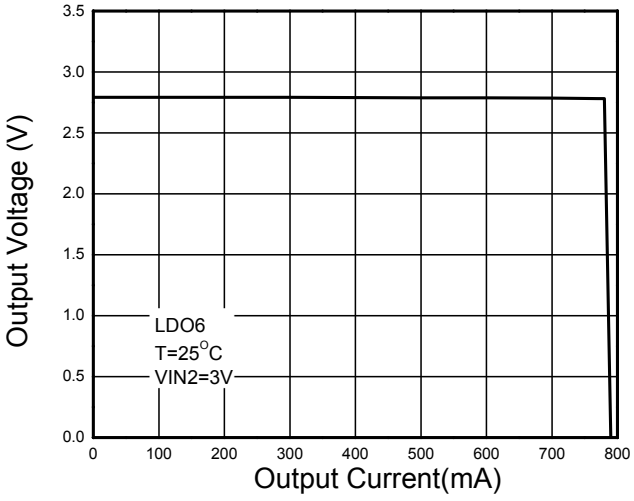
Output Voltage vs. Output Current



Output Voltage vs. Output Current



Output Voltage vs. Output Current



Output Voltage vs. Output Current

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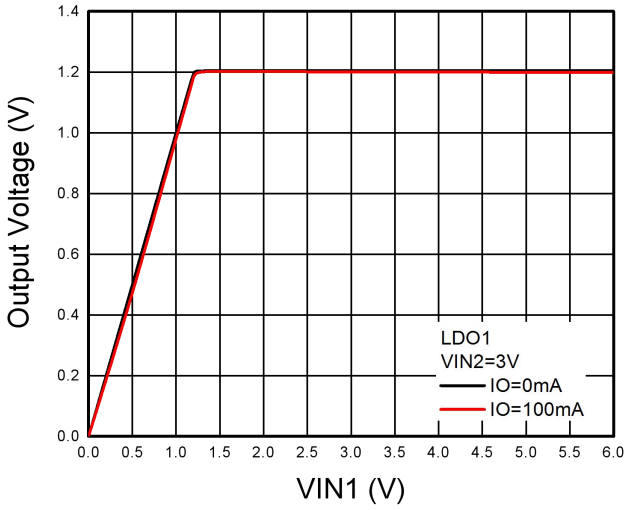
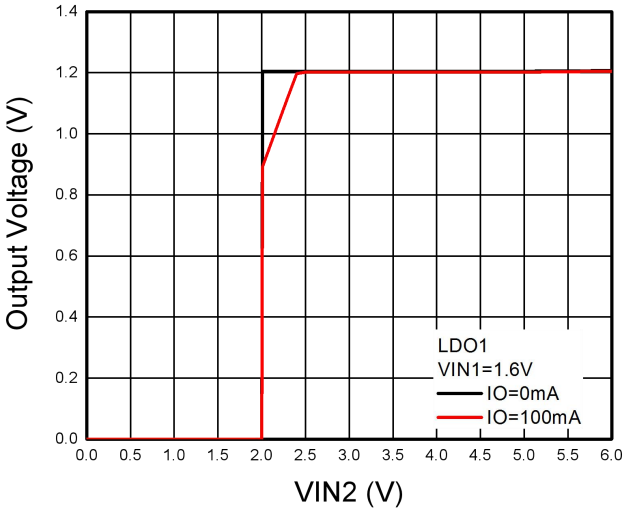
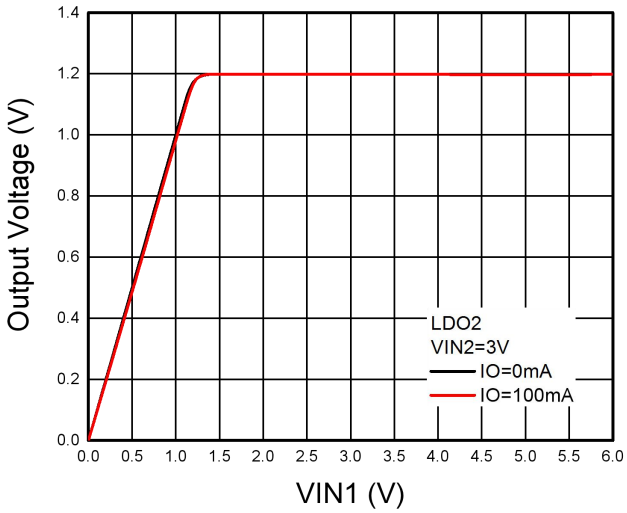
Output Voltage



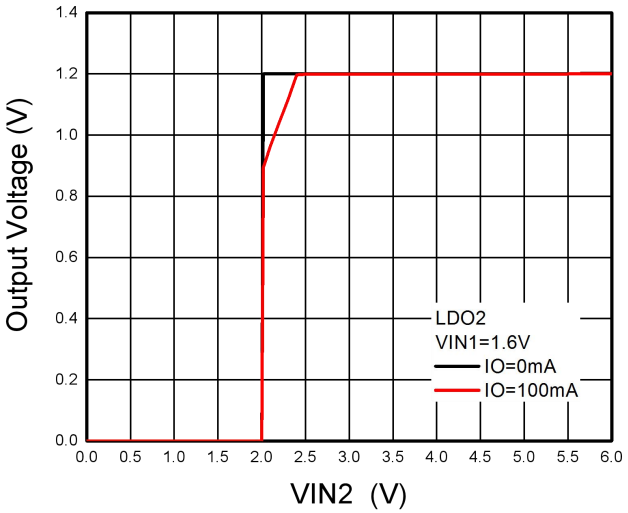
Output Voltage vs. Input Voltage1



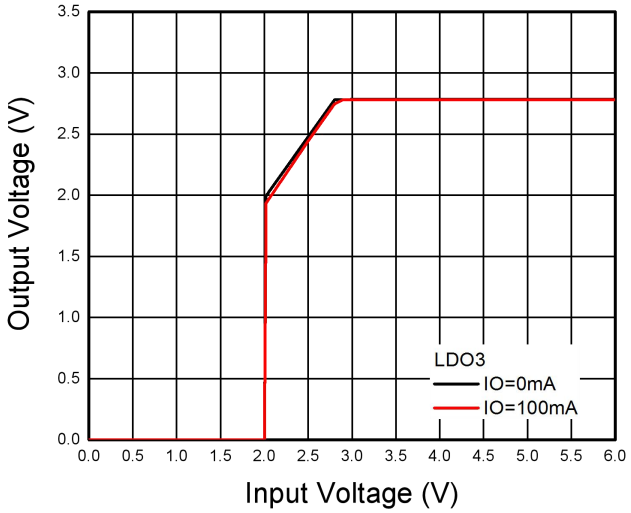
Output Voltage vs. Input Voltage 2



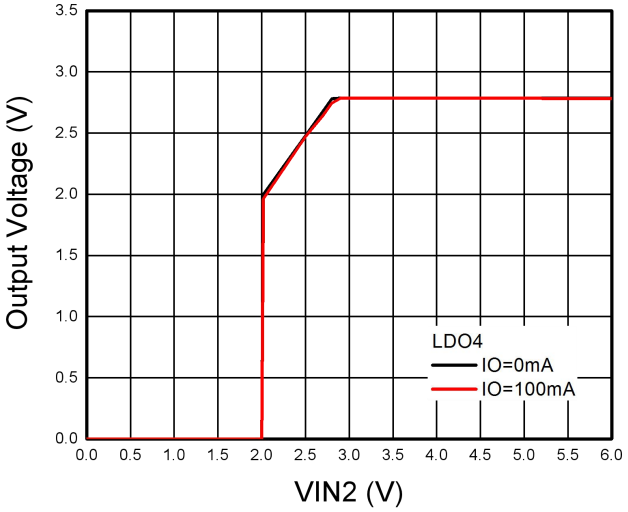
Output Voltage vs. Input Voltage 1



Output Voltage vs. Input Voltage 2



Output Voltage vs. Input Voltage 2



Output Voltage vs. Input Voltage 2

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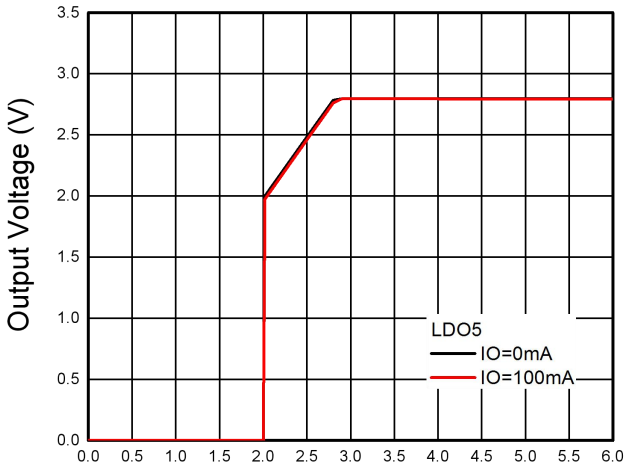
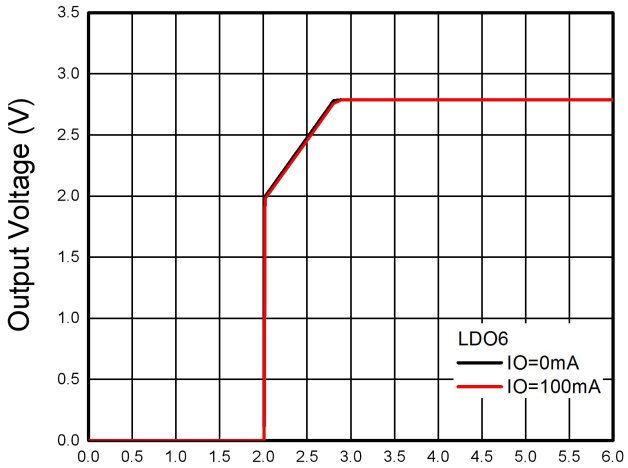
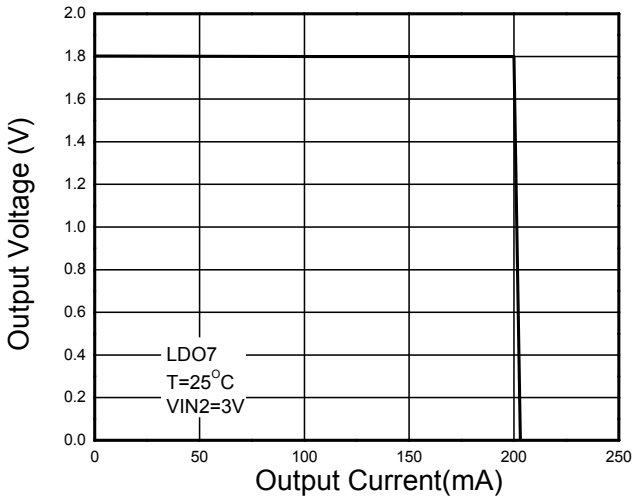


Output Voltage vs. Input Voltage 2

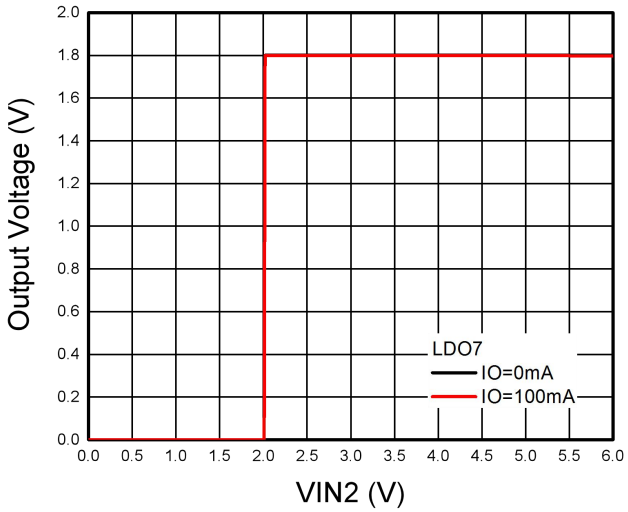


Output Voltage vs. Input Voltage 2

LDO7 Output current and output voltage



Output Voltage vs. Output Current



Output Voltage vs. Input Voltage 2

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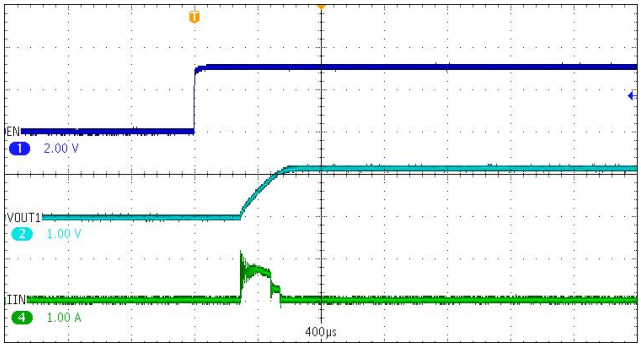
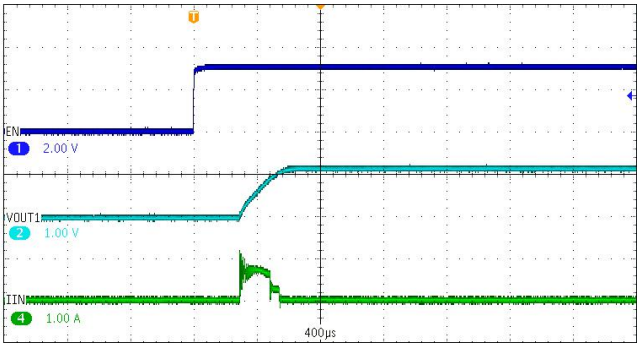
Input Inrush Current (Start-up from EN, All LDO output enable at same time)

VIN1 Inrush Current (LDO1 Cout=2.2uF, LDO2 Cout=2.2uF, Total Cout=4.4uF)

IN1 Inrush Current, Iout=0mA

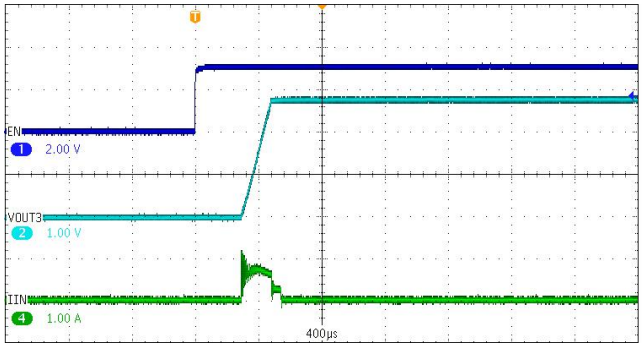


IN1 Inrush Current, Iout=100mA

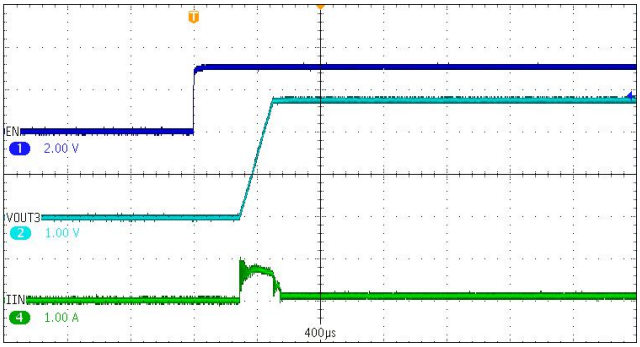


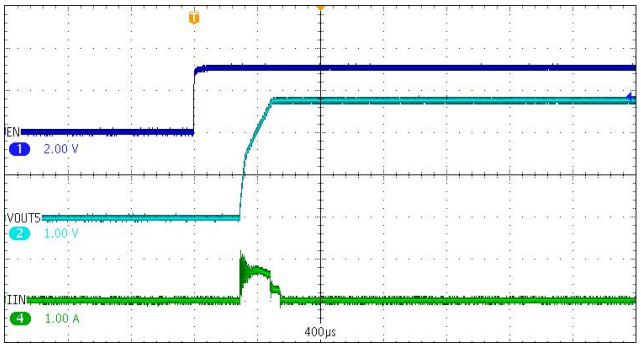
VIN2 Inrush Current (LDO3/4 Cout=1uF, LDO5/6 Cout=2.2uF, LDO7 Cout=1uF, Total Cout=7.4uF)

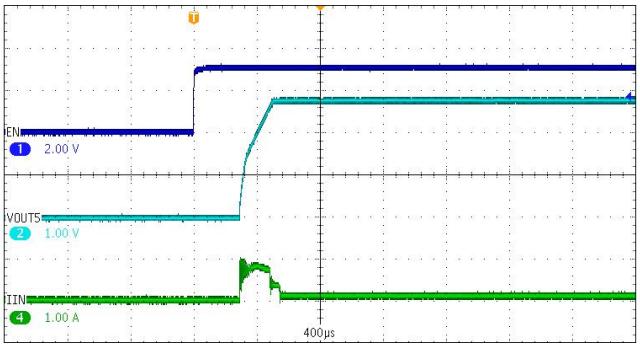
IIN2 Inrush Current, Iout=0mA

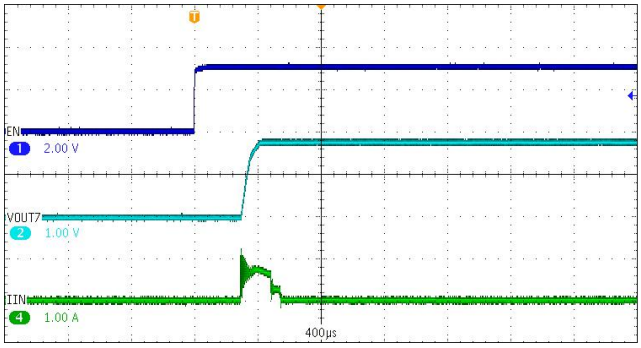


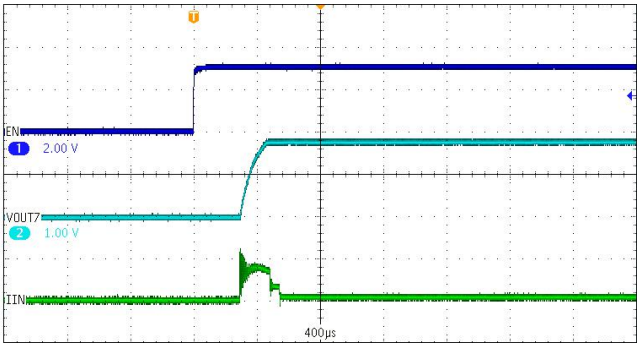
IIN2 Inrush Current, Iout=100mA











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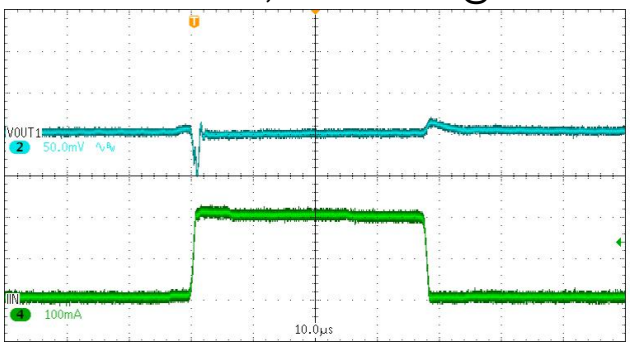
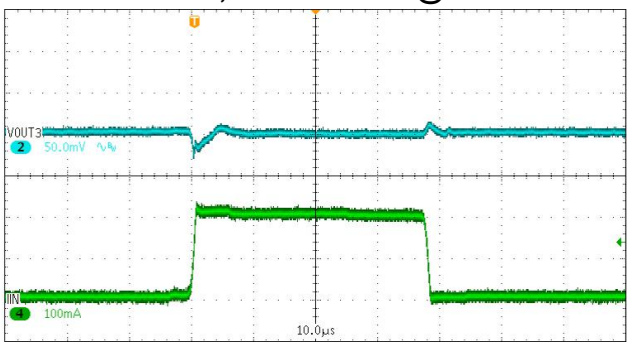
Load Transient

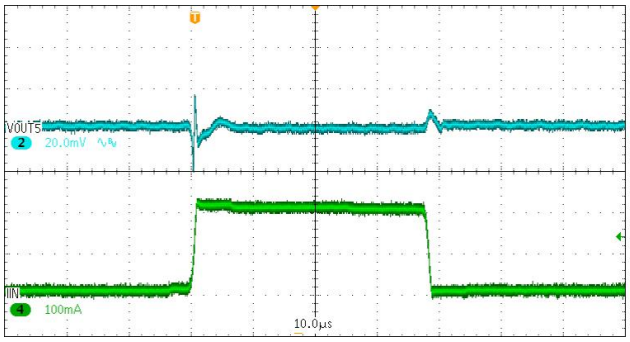
LDO1/2, Iout=1~200mA@1us



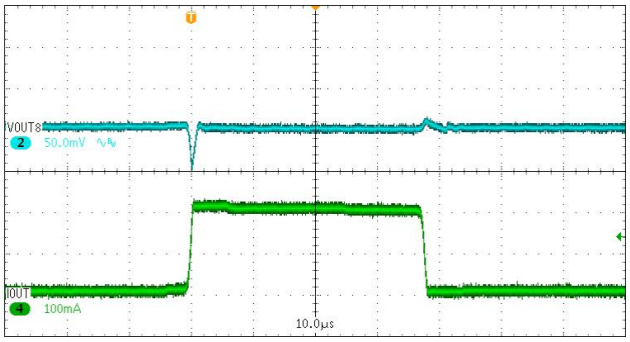
LDO3/4, Iout=1~200mA@1us



LDO 5/6, Iout=1~200mA@1us

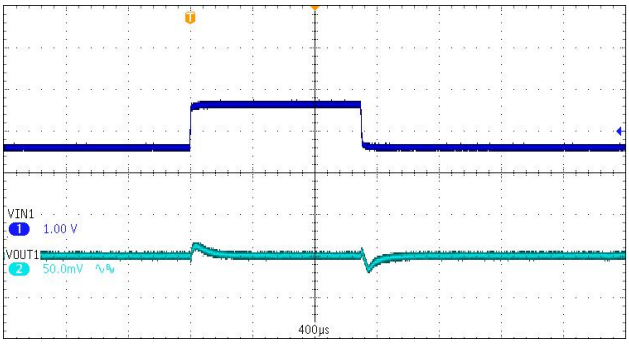


LDO7, Iout=1~200mA@1us

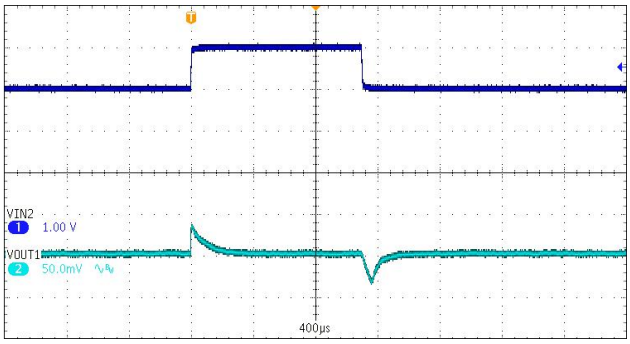


Line Transient

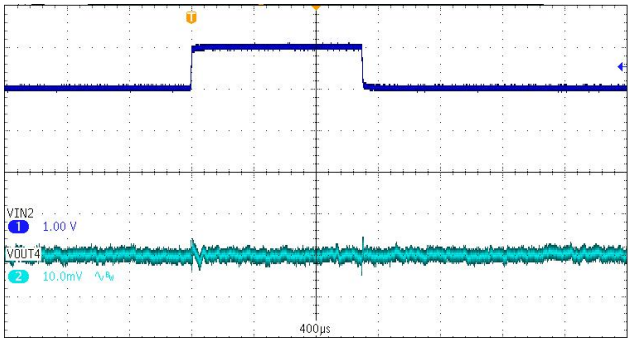
LDO1/2, VIN1=1.6~2.6V, VIN2=3V, Iout=1mA



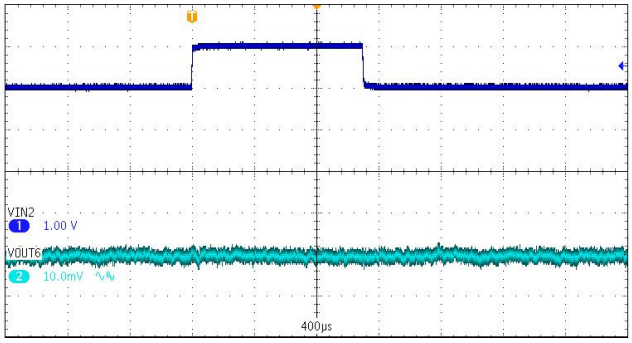
LDO1/2, VIN1=1.6V, VIN2=3~4V, Iout=1mA



LDO3/4, VIN=3~4V, Iout=1mA



LDO5/6, VIN=3~4V, Iout=1mA



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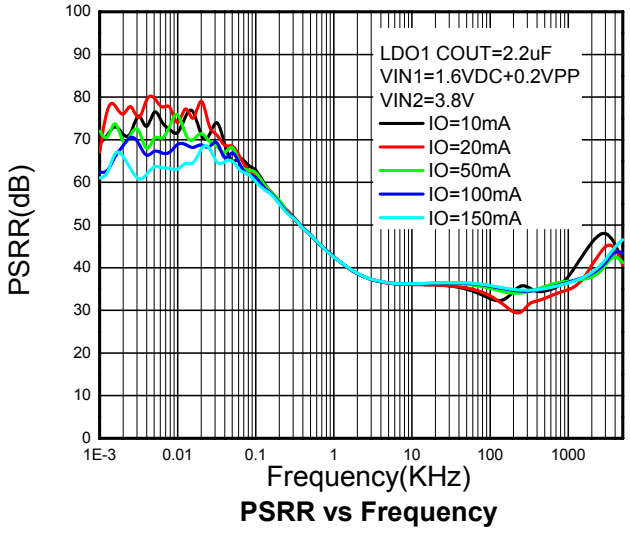
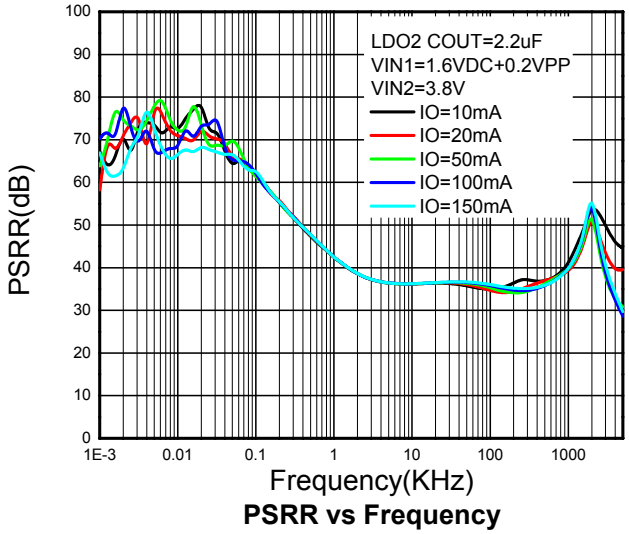
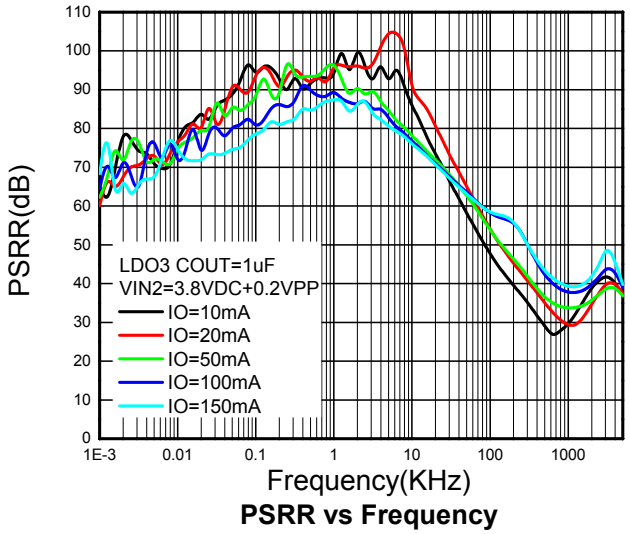
Power Supply Ripple Rejection (PSRR)



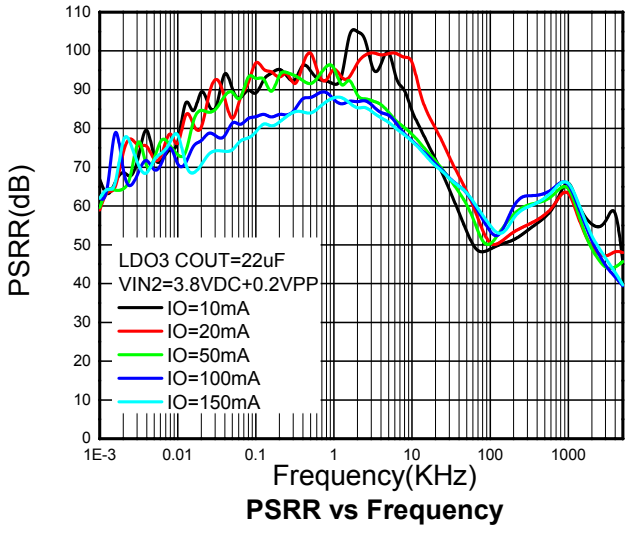
PSRR vs Frequency



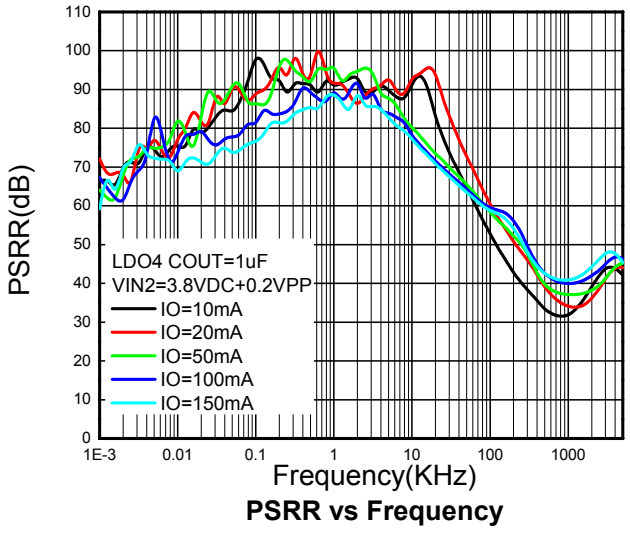
PSRR vs Frequency



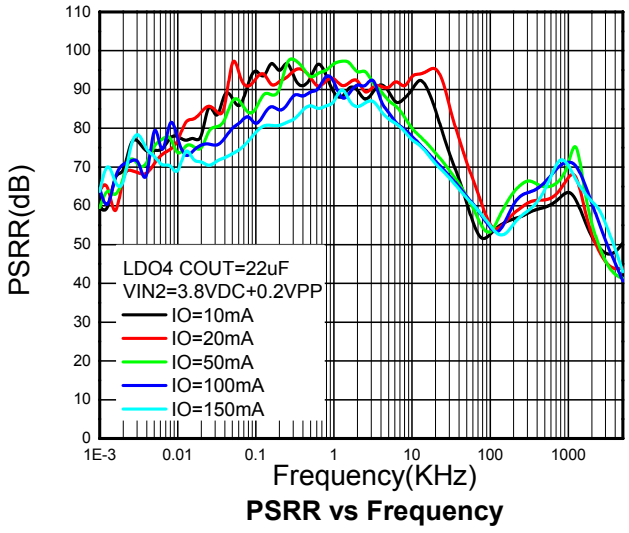
PSRR vs Frequency



PSRR vs Frequency



PSRR vs Frequency



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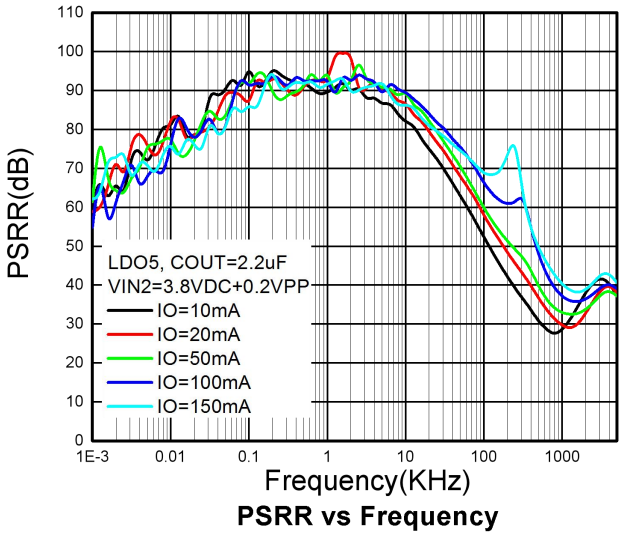
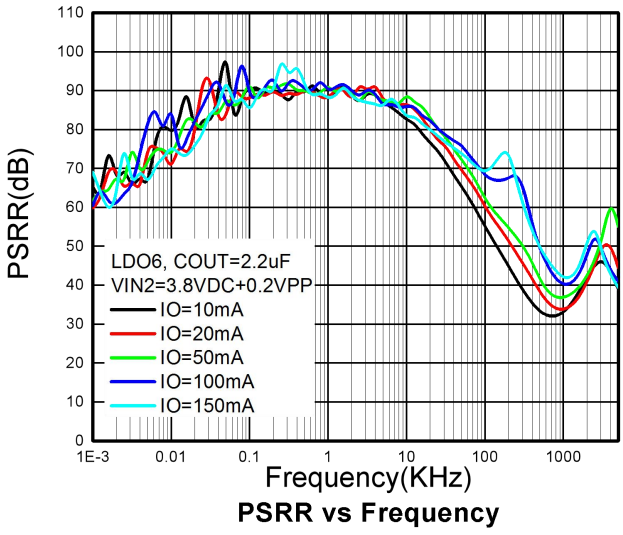
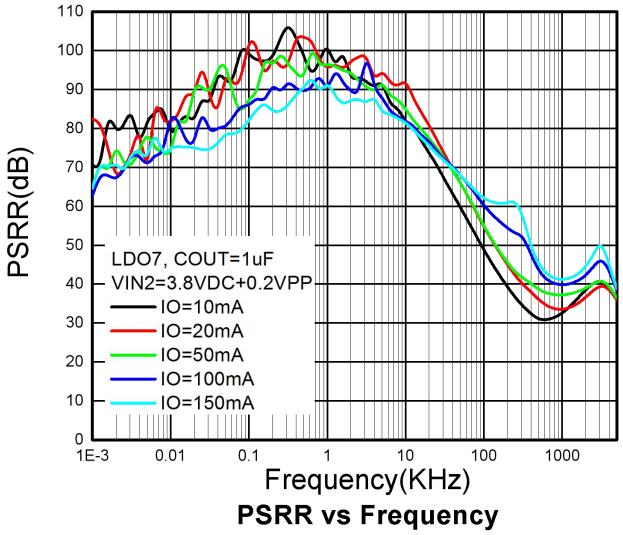


PSRR vs Frequency



PSRR vs Frequency



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Function Description

WL2864C has 7 LDO regulators. Power up/down of each regulator can be controlled by the following three ways. It can be set at the registers LDOx_SEQ[3:0] (x=1 to 7) respectively.

A. External EN pin toggles from low to high, it will force all 7 LDO regulators powered up.

B. Individual on/off control.

C. Automatic power up/down sequence control.

A. Chip enable control

External EN pin toggles from low to high, it will force all 7 LDO regulators powered up, output voltage of each LDO is default voltage, check EC Table.

When external EN pin is low, LDO output can be controlled by an I2C register.

B. Individual on/off control.

Power-up and shut down of each regulator can be controlled by an I2C register. LDOx_EN is an internal signal to enable one of regulators, If LDOx_SEQ[3:0] set to ‘0000’, that LDOx channel can be controlled directly by a bit specified in register LDOx_EN[6:0]. LDOx_VOUT[7:0] can set output voltage of each channel.

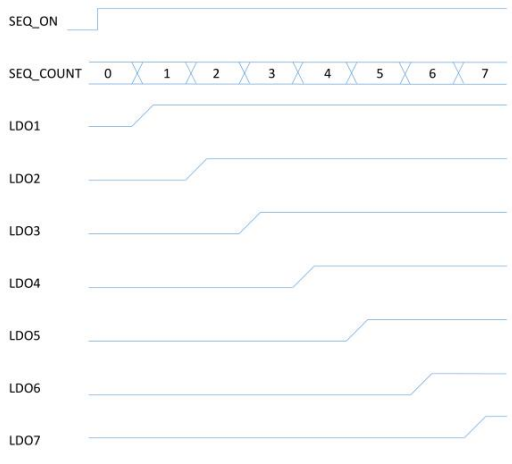
C. Automatic power up/down sequence control.

WL2864C has seven SLOTs to which each regulator can be assigned.

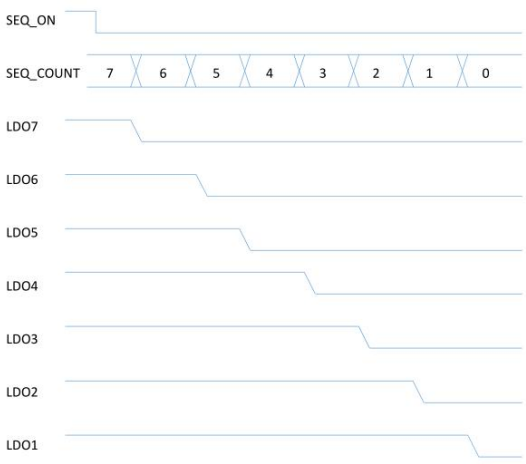
SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7

They are started by SEQ_ON signal. when SEQ_ON is high. Internal counter SEQ_COUNT[2:0] starts increments from 0 (“000”) to 7 (“111”). When SEQ_ON is low, SEQ_COUNT[2:0] decrements from 7 (“111”) to 0 (“000”). Regulators assigned to one of SLOTs starts power-up or power-down when SEQ_COUNT[2:0] matches the SLOT number.

Internal logic signal SEQ_ON is asserted by I2C, write ‘00’ to SEQ_CTRL[1:0] will set SEQ_ON to ‘0’, while write ‘01’ to SEQ_CTRL[1:0] will set SEQ_ON to ‘1’.



Example of Power-up in the case of LDO1 – LDO7 are assigned to SLOT1 – SLOT7 respectively



Example of Shutdown in the case of LDO1 – LDO7 are assigned to SLOT1 – SLOT7 respectively.

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Current limit setting

Set related bits to select Current limit threshold with 0x01H Register. Check detail information at register map and register descriptions section.

Output discharge setting

Set related bits to select output discharge function for Discharge Resistor(0x02H Register), “0”: Enable. “1”: Disable.

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I2C Interface

WL2864 utilizes I2C interface to write / read internal registers. It supports 100Kbps standard mode 400Kbps fast mode. The I2C address is 0x52H.

I2C Serial Data Bus

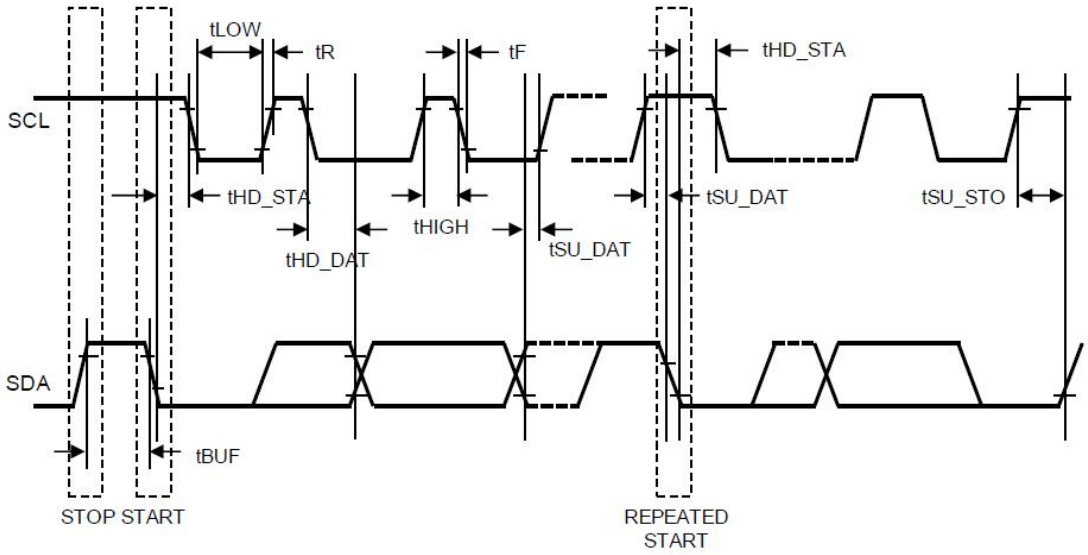

Figure 2. I²C Mode Timing Diagram

The WL2864 supports the I2C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. The WL2864 operates as a slave on the I2C bus. Within the bus specifications a standard mode (100kHz maximum clock rate) and a fast mode (400kHz maximum clock rate) are defined. The WL2864 works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The following bus protocol has been defined (Figure 2 and Figure 3). Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period

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of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

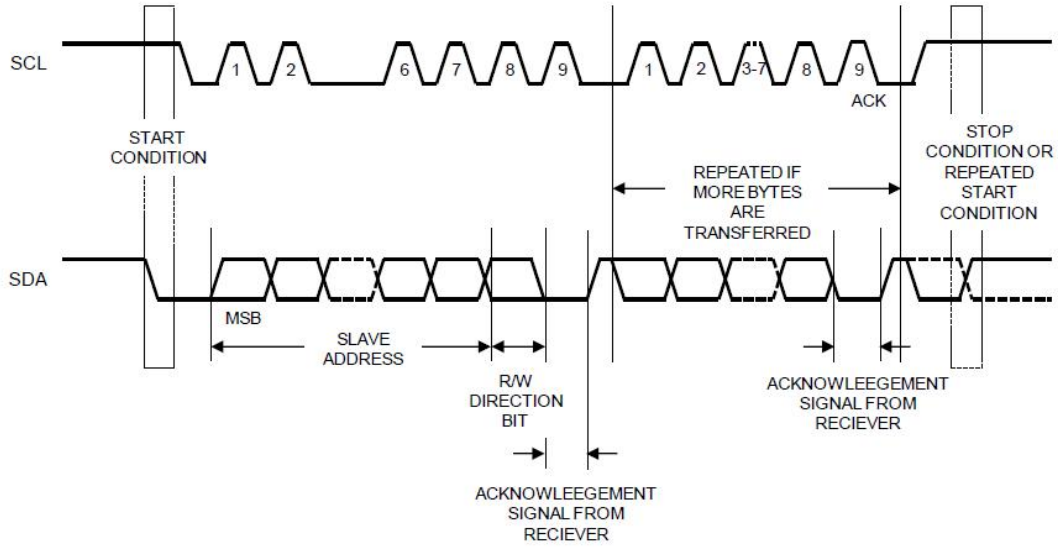

Figure 3. Data Transfer on I²C Serial Bus

Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

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The WL2864 can operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 4 for Interface). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7- WL2864 address followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. After the WL2864 acknowledges the slave address + write bit, the master transmits a register address to the WL2864. This sets the register pointer on the WL2864. The master may then transmit zero or more bytes of data, with the WL2864 acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2. Slave Transmitter Mode (Read Mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the WL2864 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit WL2864 address followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs an acknowledge on the SDA line. The WL2864 then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The WL2864 must receive a “not acknowledge” to end a read.

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The 7-bit slave device address is 0101001 binary (or 52H).

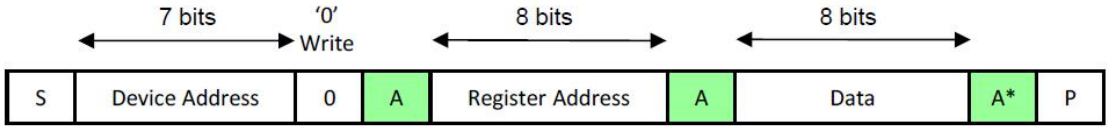

Figure 4. I²C Write – Slave Receiver Mode

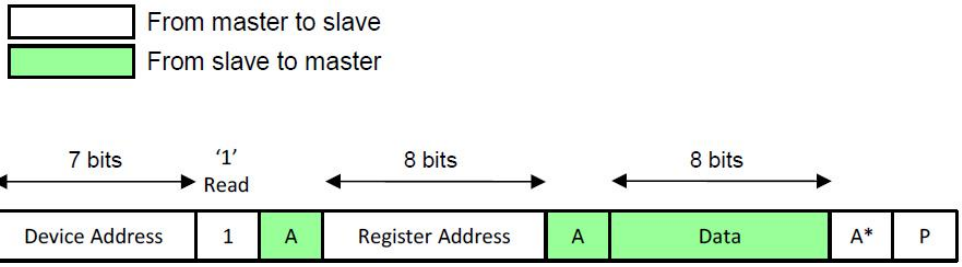

Figure 5. I²C Read – Slave Transmitter Mode

Where

S	= START condition
P	= STOP condition
Device Address	= 0101001 (7 bits, MSB first)
Register Address	= Reg0 – Reg15 address (8 bits)
Data	= data to read or write (8 bits)
1	= Read command bit
0	= Write command bit
A	= acknowledge (SDA low)
A*	= not acknowledge (SDA high)

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Register Map

0x00	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Chip_REV[7:0]							
Mode	R							
Init	0000 0001							
0x01	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		LDO7_CL	LDO5/6_CL[1:0]		LDO3/4_CL[1:0]		LDO1/2_CL[1:0]	
Mode		RW	RW		RW		RW	
Init		0	00		00		00	
0x02	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		Discharge Resistor Selection						
Mode		RW						
Init		000 0000						
0x03	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO1_VOUT[7:0]							
Mode	RW							
Init	0011 0000							
0x04	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO2_VOUT[5:0]							
Mode	RW							
Init	0011 0000							
0x05	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO3_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x06	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO4_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x07	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO5_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x08	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO6_VOUT[7:0]							
Mode	RW							
Init	1000 0000							

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0x09	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO7_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x0A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO2_SEQ[3:0]				LDO1_SEQ[3:0]			
Mode	RW				RW			
Init	0000				0000			
0x0B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO4_SEQ[3:0]				LDO3_SEQ[3:0]			
Mode	RW				RW			
Init	0000				0000			
0x0C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO6_SEQ[3:0]				LDO5_SEQ[3:0]			
Mode	RW				RW			
Init	0000				0000			
0x0D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name					LDO7_SEQ[3:0]			
Mode					RW			
Init					0000			
0x0E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		LDOx_EN						
Mode		RW						
Init		000 0000						
0x0F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SEQ_SPEED[1:0]		SEQ_CTRL[1:0]		SEQ_ON	SEQ_COUNT[2:0]		
Mode	RW		RW		R	R		
Init	00		00		0	000		

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Register Description

0x00	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	Chip_REV[7:0]							
Mode	R							
Init	0000 0001							

Chip_REV[7:0]

Indicates the device ID with revision. Read only.

0x01	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		LDO7_CL	LDO5/6_CL[1:0]		LDO3/4_CL[1:0]		LDO1/2_CL[1:0]	
Mode		RW	RW		RW		RW	
Init		0	00		00		00	

Current Limit Selection

Defined the typical value of current limit threshold for each LDOs.

Register LDO1/2_CL[1:0] is for LDO1 and LDO2; Register LDO3/4_CL[1:0] is for LDO3 and LDO4;

Register LDO5/6_CL[1:0] is for LDO5 and LDO6; Register LDO7-CL is for LDO7

The detail current limit value are shown in the table as below

Register Name	Register Value	Current Limit Threshold (mA)
LDO1/2_CL[1:0]	00	900
	01	750
	10	960
	11	950
LDO3/4_CL[1:0]	00	550
	01	450
	10	700
	11	650
LDO5/6_CL[1:0]	00	900
	01	800
	10	950
	11	920
LDO7_CL	0	220
	1	300

0x02	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		Discharge Resistor Selection						
Mode		RW						
Init		000 0000						

Discharge Resistor Selection

Each LDO regulators output discharge resistor enable control. Bit0 for LDO1, ~~ Bit6 for LDO7

0=Enable, 1=Disable.

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0x03	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO1_VOUT[7:0]							
Mode	RW							
Init	0011 0000							
0x04	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO2_VOUT[5:0]							
Mode	RW							
Init	0011 0000							

LDO1_VOUT[7:0] & LDO2_VOUT[7:0]

Define the Output Voltage Level of LDO1 & LDO2

$VOUT_X = 0.6V + LDO_X\_VOUT[7:0] * 0.0125V$

The following table shown the code of each voltage setting for reference

Dec.	Binary	Hex.	Voltage (V)	Dec.	Binary	Hex.	Voltage (V)
0	0000 0000	00H	0.6000	26	0001 1010	1AH	0.9250
1	0000 0001	01H	0.6125	27	0001 1011	1BH	0.9375
2	0000 0010	02H	0.6250	28	0001 1100	1CH	0.9500
3	0000 0011	03H	0.6375	29	0001 1101	1DH	0.9625
4	0000 0100	04H	0.6500	30	0001 1110	1EH	0.9750
5	0000 0101	05H	0.6625	31	0001 1111	1FH	0.9875
6	0000 0110	06H	0.6750	32	0010 0000	20H	1.0000
7	0000 0111	07H	0.6875	33	0010 0001	21H	1.0125
8	0000 1000	08H	0.7000	34	0010 0010	22H	1.0250
9	0000 1001	09H	0.7125	35	0010 0011	23H	1.0375
10	0000 1010	0AH	0.7250	36	0010 0100	24H	1.0500
11	0000 1011	0BH	0.7375	37	0010 0101	25H	1.0625
12	0000 1100	0CH	0.7500	38	0010 0110	26H	1.0750
13	0000 1101	0DH	0.7625	39	0010 0111	27H	1.0875
14	0000 1110	0EH	0.7750	40	0010 1000	28H	1.1000
15	0000 1111	0FH	0.7875	41	0010 1001	29H	1.1125
16	0001 0000	10H	0.8000	42	0010 1010	2AH	1.1250
17	0001 0001	11H	0.8125	43	0010 1011	2BH	1.1375
18	0001 0010	12H	0.8250	44	0010 1100	2CH	1.1500
19	0001 0011	13H	0.8375	45	0010 1101	2DH	1.1625
20	0001 0100	14H	0.8500	46	0010 1110	2EH	1.1750
21	0001 0101	15H	0.8625	47	0010 1111	2FH	1.1875
22	0001 0110	16H	0.8750	**48**	**0011 0000**	**30H**	**1.2000**
23	0001 0111	17H	0.8875	49	0011 0001	31H	1.2125
24	0001 1000	18H	0.9000	50	0011 0010	32H	1.2250
25	0001 1001	19H	0.9125	~255	******		

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0x05	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO3_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x06	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO4_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x07	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO5_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x08	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO6_VOUT[7:0]							
Mode	RW							
Init	1000 0000							
0x09	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO7_VOUT[7:0]							
Mode	RW							
Init	1000 0000							

LDO3_VOUT[7:0] to LDO7_VOUT[7:0]

Define the Output Voltage Level of LDO3 to LDO7

$VOUT_X$ = 1.2V + LDO_X_VOUT[7:0] * 0.0125V.

The following table shown the code of each voltage setting for reference

Dec.	Binary	Hex.	Voltage (V)	Dec.	Binary	Hex.	Voltage (V)
0	0000 0000	00H	1.2000	**128**	**1000 0000**	**80H**	**2.8000**
1	0000 0001	01H	1.2125	129	1000 0001	81H	2.8125
2	0000 0010	02H	1.2250	130	1000 0010	82H	2.8250
3	0000 0011	03H	1.2375	131	1000 0011	83H	2.8375
4	0000 0100	04H	1.2500	132	1000 0100	84H	2.8500
5	0000 0101	05H	1.2625	133	1000 0101	85H	2.8625
6	0000 0110	06H	1.2750	134	1000 0110	86H	2.8750
7	0000 0111	07H	1.2875	135	1000 0111	87H	2.8875
8	0000 1000	08H	1.3000	136	1000 1000	88H	2.9000
9	0000 1001	09H	1.3125	137	1000 1001	89H	2.9125
10	0000 1010	0AH	1.3250	138	1000 1010	8AH	2.9250
11	0000 1011	0BH	1.3375	139	1000 1011	8BH	2.9375
12~127	******			~255	******		

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0x0A	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO2_SEQ[3:0]				LDO1_SEQ[3:0]			
Mode	RW				RW			
Init	0000				0000			
0x0B	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO4_SEQ[3:0]				LDO3_SEQ[3:0]			
Mode	RW				RW			
Init	0000				0000			
0x0C	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	LDO6_SEQ[3:0]				LDO5_SEQ[3:0]			
Mode	RW				RW			
Init	0000				0000			
0x0D	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name					LDO7_SEQ[3:0]			
Mode					RW			
Init					0000			

LDOx_SEQ[3:0]

Power sequence setting register. there are 7 time slots defined as following table. The power-up sequence is start from slot1 to slot7, and shut down start from slot7 to slot1. Power-up and shut down of each LDO regulator can be set at any one of the slots.

Register Value	VOUTx
0000	Controlled by I2C register LDOx_EN[6:0]
x001	slot1
x010	slot2
x011	slot3
x100	slot4
x101	slot5
x110	slot6
x111	slot7

In the case of that register value of LDOx_SEQ[3:0] are set to be default “0000”, that LDO regulators will be controlled by register LDOx_EN[6:0]. Otherwise, which will be controlled by register SEQ_CTRL[1:0], in this stage, the power-up and shutdown sequence of each LDO regulators will be followed by register LDOx_SEQ[3:0] setting witch shown as above table.

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0x0E	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name		LDOx_EN						
Mode		RW						
Init		000 0000						

LDOx_EN

Chip enable control register by I2C while the register value of LDOx_SEQ[3:0] are set to be default "0000". This register can be written to enable or disable the corresponding LDO regulator. Bit0 for LDO1, ~~ Bit6 for LDO7.

0x0F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Name	SEQ_SPEED[1:0]		SEQ_CTRL[1:0]		SEQ_ON	SEQ_COUNT[2:0]		
Mode	RW		RW		R	R		
Init	00		00		0	000		

SEQ_SPEED[1:0] define the slot period as following:

Register Value	slot period (ms)
00	2.00
01	1.00
10	0.50
11	0.25

SEQ_CTRL[1:0] enables power-up or shut down of SEQ

Register Value	SEQ Status
x0	Shutdown
x1	Power-up

SEQ_ON[1:0] indicates the activation signal of SEQ, read only.

Register Value	SEQ Status
0	Shutdown
1	Power-up

SEQ_COUNT[1:0] indicates the slot number of SEQ at the moment. Read only.

Register Value	SEQ Counter
000	No LDO starts.
001	slot1 starts
010	slot2 starts
011	slot3 starts
100	slot4 starts
101	slot5 starts
110	slot6 starts
111	slot7 starts and stop counting.

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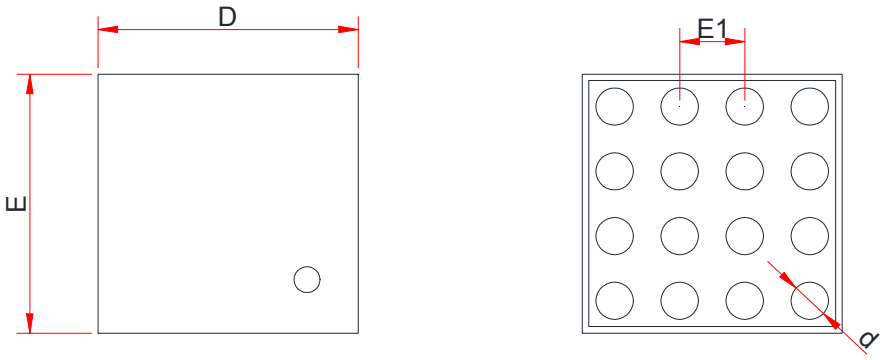
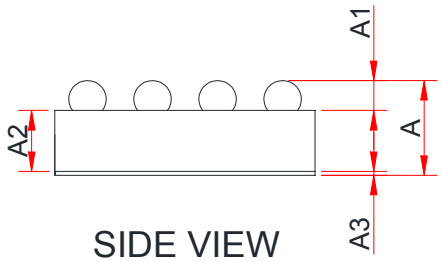
PACKAGE OUTLINE DIMENSIONS

CSP-16L



TOP VIEW

BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Min.
A	0.55	-	0.62
A1	0.16	-	0.21
A2	0.36	-	0.39
A3	0.03Typ.		
D	1.54	1.57	1.60
E	1.54	1.57	1.60
E1	0.40 Typ.		
d	0.21	0.23	0.25

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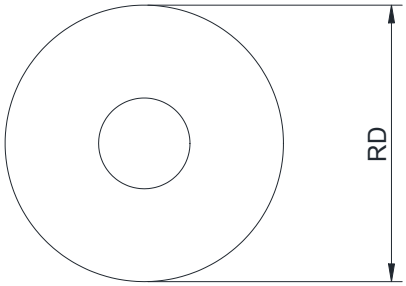
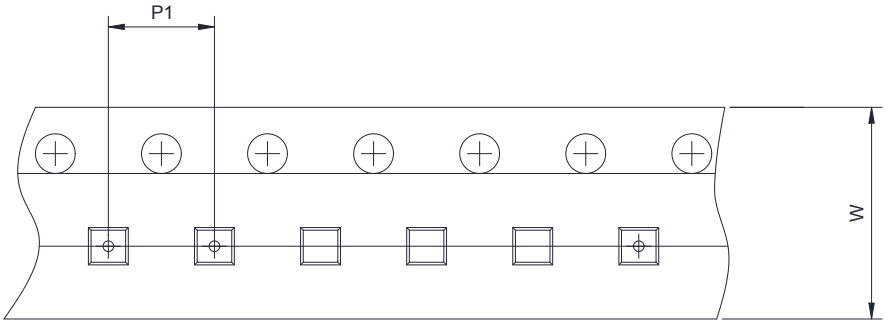
TAPE AND REEL INFORMATION

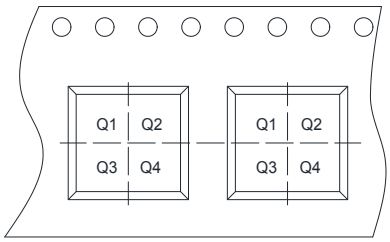
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



User Direction of Feed

RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4

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