WD31089Q

12.6V, 7A Fully-Integrated Synchronous Boost Converter

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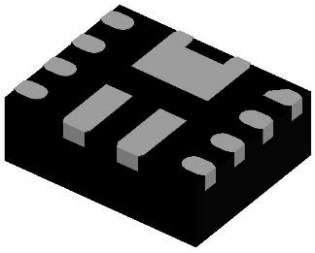
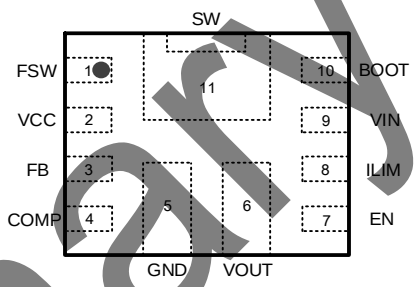
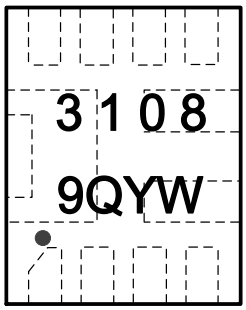


QFN2520-12L



Pin configuration (Top view)



3108 = Device code
9Q = Special code
Y = Year code
W = Week code

Marking

Descriptions

The WD31089 is a fully-integrated synchronous boost converter. The device provides a high efficiency and small size power solution for portable equipment. The WD31089 features wide input voltage range from 2.7V to 12V to support applications powered with single cell or two cell Lithium ion/polymer batteries. The WD31089 has 7A continuous switch current capability and provides output voltage up to 12.6V.

The WD31089 uses adaptive constant off-time peak current mode control to regulate the output voltage. The switching frequency in the PWM mode is adjustable from 200kHz to 2.2MHz. The WD31089 also implements a built-in 4ms soft start function and an adjustable peak switch current limit function. In addition, the device provides 13.2V output overvoltage protection, cycle-by-cycle overcurrent protection, and thermal shutdown protection.

The WD31089 is available in a 2.0mm×2.5mm QFN2520-12L package. Standard products is Pb-Free and Halogen-Free.

Features

- Input Voltage Range of 2.7V to 12V
- Output Voltage Range: 4.5 V to 12.6 V
- Integrate 19mΩ (Power Switch) / 27mΩ (Rectifier Side)
- Up to 90% EFF at V_{IN} = 3.3 V, V_{OUT} = 9 V, I_{OUT} = 2 A
- Adjustable Switching Frequency: 200kHz to 2.2MHz
- Resistor-Programmable Peak Current Limit up to 10A for high pulse current and Hiccup
- Power Save Mode at Light Load
- Fast Load Transient Response with COT Control Mode
- Internal Output Overvoltage Protection at 13.2 V
- Thermal Shutdown

Applications

- Bluetooth™ Speaker
- Quick Charge Power Bank
- Portable POS Terminal
- E-Cigarette

Order information

Device	Package	Shipping
WD31089Q-12/TR	QFN2520-12L	3000/Reel&Tape

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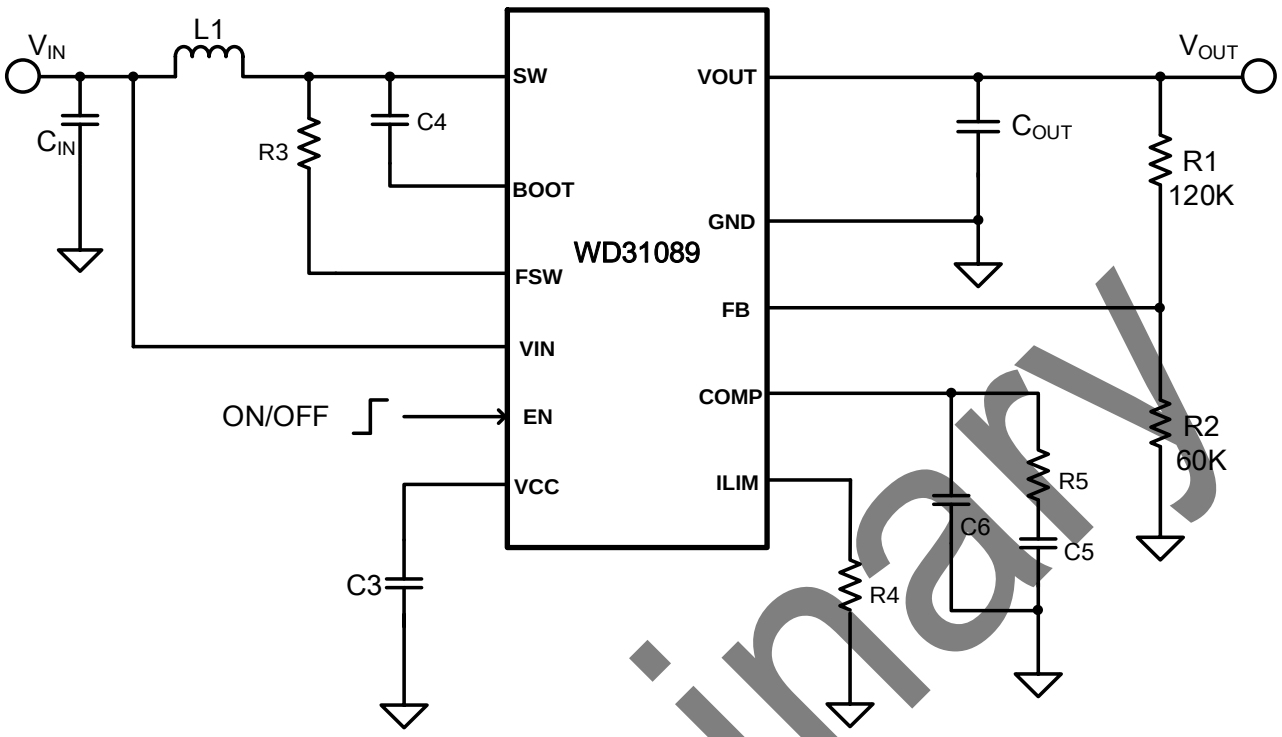
Typical Applications



Pin Descriptions

No.	Symbol	Description
1	FSW	Switching frequency is programmed by a resister between this pin and the SW pin.
2	VCC	Output of the internal regulator. A ceramic capacitor of more than 1.0 µF is required between this pin and ground.
3	FB	Output voltage feedback.
4	COMP	Output of the internal trans-conductance amplifier, the loop compensation network should be connected between this pin and the GND pin.
5	GND	Ground.
6	VOUT	Converter output.
7	EN	Enable input control pin. High logic enables the device and low logic disables the device.
8	ILIM	Peak current limit programmed by a resister between this pin and the GND pin.
9	VIN	Supply Voltage pin. Requires a ceramic cap of 0.1uF or more is required between this pin and ground.
10	BOOT	Bootstrap pin. Connect a 0.1uF capacitor between this pin and SW pin
11	SW	Switching node.

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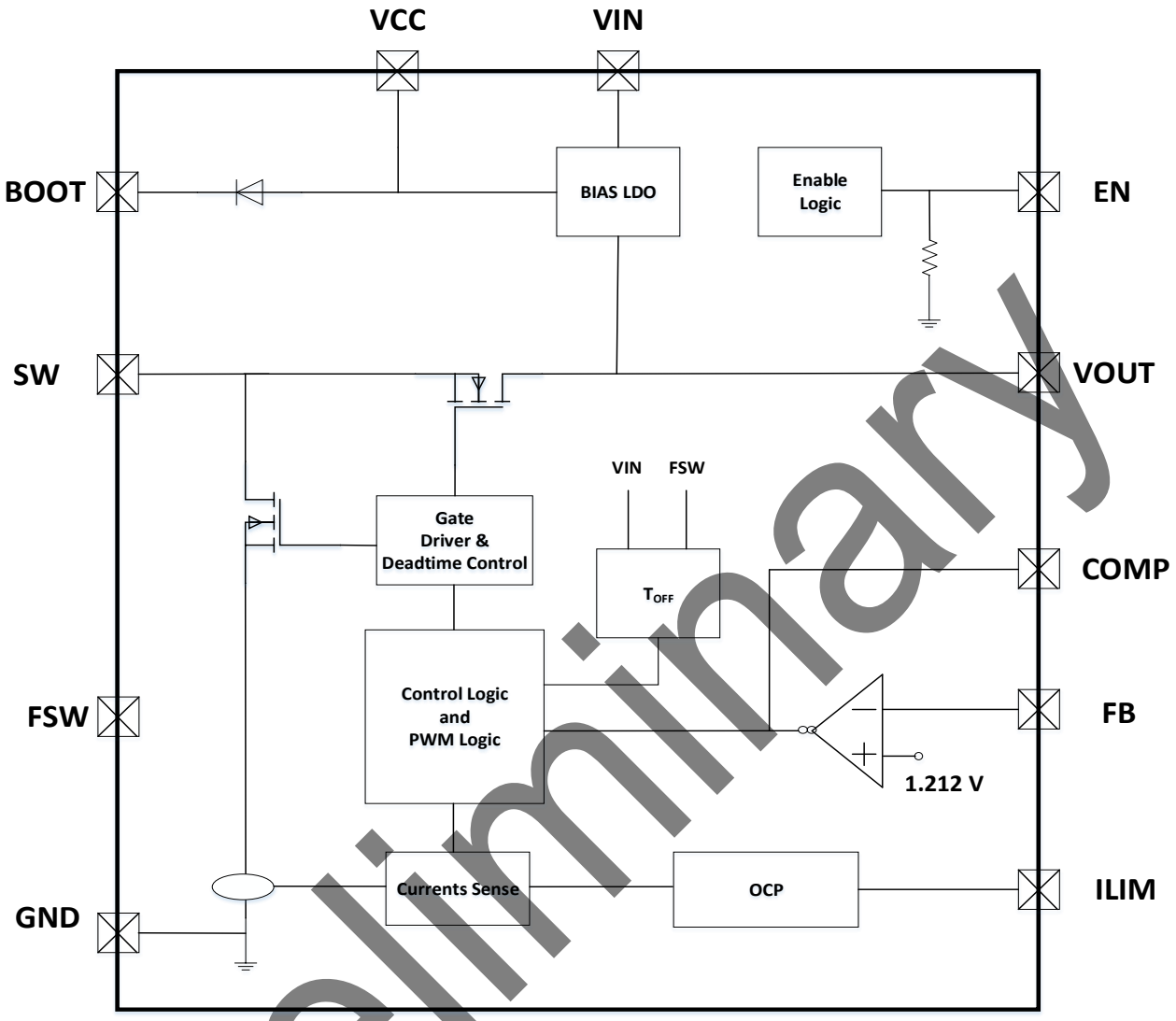
Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
VIN, SW, FSW, VOUT Pin Voltage Range	-	-0.3～+14.5	V
EN, VCC, COMP, ILIM, FB Pin Voltage Range	-	-0.3～6	V
BOOT Pin Voltage Range(DC)		(V_{SW}– 0.3) ~ (V_{SW} + 6)	V
Thermal Characteristics (1)	$R_{\theta JA}$	53.4	°C/W
	$R_{\theta JC}$	59.2	°C/W
Maximum Junction Temperature	T_J	150	°C
Lead Temperature(Soldering, 10s)	T_L	260	°C
Operating Ambient Temperature	Topr	-40 ~ 85	°C
Storage Temperature	Tstg	-65 ~ 150	°C
ESD Classification	HBM		V
	CDM		V

Recommended Operation Conditions (2)

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Symbol	Characteristics	Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage	2.7		12	V
V_{OUT}	Output Voltage	4.5		12.6	V
L	Inductance, effective value	0.47	2.2	10	μH
C_{IN}	Input capacitance, effective value	10			μF
C_{OUT}	Output capacitance, effective value	10	47	1000	μF
C3	VCC decoupling cap		1.0		μF
C4	Bootstrap cap		0.1		μF
T_J	Operating junction temperature	-40	-	125	℃

These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Note 1: Surface mounted on FR-4 Board using 1 square inch pad size, dual side, 1oz copper.

Note 2: The device is not guaranteed to function outside of its operating conditions.

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Electronics Characteristics

V_{IN} = 2.7 V to 5.5 V, V_{OUT} = 9 V, T_J = –40°C to 125°C. Typical values are at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
POWER SUPPLY						
Input Voltage Range	V_{IN}		2.7		12	V
V_{IN} Under Voltage Lockout Threshold	V_{UVLO}	Rising			2.7	V
		Falling		2.4	2.5	
V_{IN} UVLO Hysteresis	V_{IN_HYS}			200		mV
VCC Regulation Voltage	V_{CC}	ICC = 2 mA, VIN = 8 V		5.5		V
VCC UVLO Threshold	V_{CC_UVLO}			2.1		V
Standby Supply Current into V_{IN}	I_Q	V_{FB} = 1.3V, I_{OUT} = 0A		10	15	µA
Standby Supply Current into V_{out}		V_{FB} = 1.3V, I_{OUT} = 0A		70	100	µA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V, Vin=5.5V		1	3	µA
OUTPUT						
Output Voltage Range	V_{out}		4.5		12.6	v
Feedback Reference Voltage	V_{FB}		-2%	1.212	2%	V
Feedback Leakage Current	I_{FB}	V_{FB}=1.3V			±100	nA
Output Overvoltage Protection Threshold	Vovp	V_{OUT} rising	12.7	13.2	13.7	v
Output Overvoltage Protection Hysteresis	V_{OVP_HYS}	V_{OUT} falling below V_{OVP}		0.25		V
Soft Startup Time	t_{ss}	C_{OUT}(effective) = 47 µF, I_{OUT} = 0 A	2	4	6	ms
ERROR AMPLIFIER						
COMP Pin Sink Current	I_{SINK}	V_{FB} = V_{REF} + 200 mV, V_{COMP} = 1.9 V		20		µA
COMP Pin Source Current	I_{SOURCE}	V_{FB} = V_{REF} – 200 mV, V_{COMP} = 1.9 V		20		µA
High Clamp Voltage at the COMP Pin	V_{CCLP_H}	V_{FB} = 1 V, R_{ILIM} = 127 kΩ		2.3		V
Low Clamp Voltage at the COMP Pin	V_{CCLP_L}	V_{FB} = 1.4 V, R_{ILIM} = 127 kΩ		1.4		V
Error Amplifier Transconductance	G_{EA}	V_{COMP} = 1.9 V		190		µS
POWER SWITCH						
$R_{DS(ON)}$ of HS FET	R_{UFET}	I_{SW} = 100mA		27	44	mΩ
$R_{DS(ON)}$ of LS FET	R_{LFET}	I_{SW} = −100mA		19	31	mΩ
SWITCHING FREQUENCY						
Oscillator Frequency	F_{SW}	R_{FSW} = 301 kΩ		500		kHz
		R_{FSW} = 46.4 kΩ		2000		kHz
Minimum On Time	t_{ON_min}	VCC = 5.5 V		90	180	ns

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Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CURRENT LIMIT						
Inductor Valley Current Limit	I_{LIM}	R_{ILIM} = 127 kΩ	7.3	8.1	8.9	A
		R_{ILIM} = 100 kΩ	9	10	11	A
Internal Reference Voltage at ILIM Pin	V_{ILIM}			1.212		V
EN LOGIC INPUT						
EN Rising Threshold	V_{ENH}				1.2	V
EN Falling Threshold	V_{ENL}		0.4			V
EN Pulldown Resistor	R_{EN}			800		kΩ
Protection						
Over Temperature Protection	T_{OTP}	T_J rising		155		°C
OTP Hysteresis	T_{OTP_HYS}	T_J falling below T_{OTP}		25		°C

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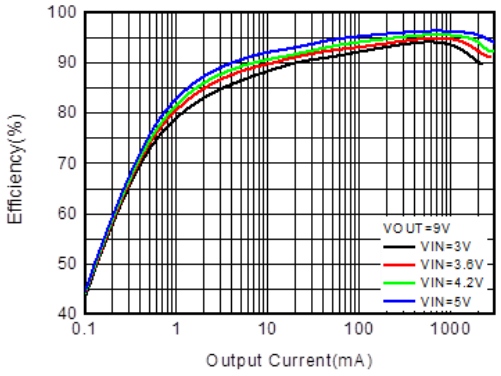
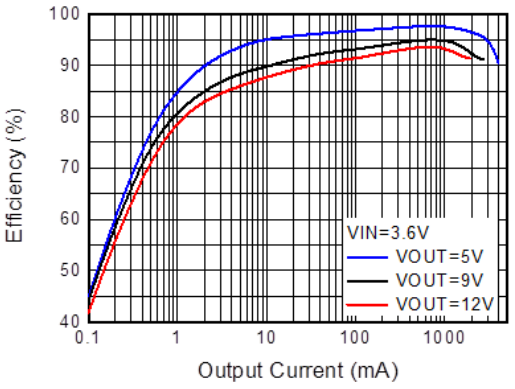
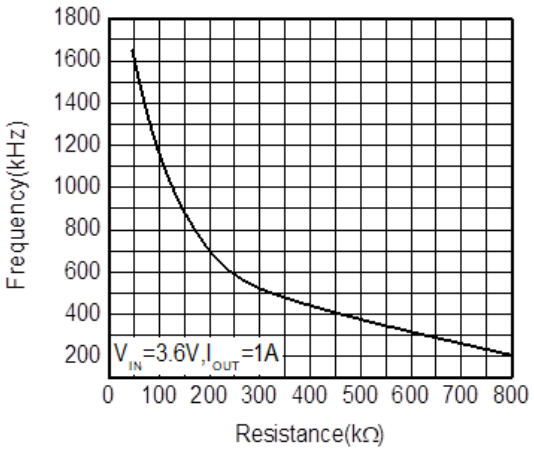
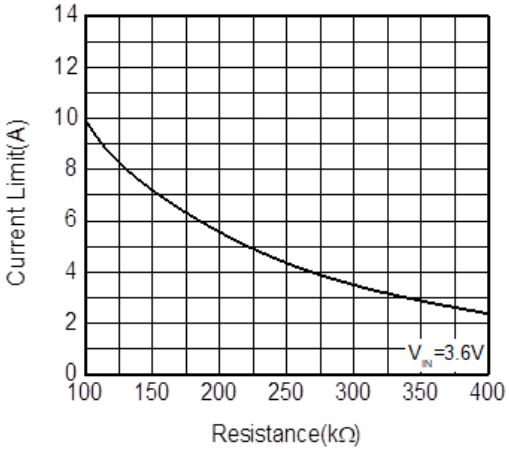
Typical Characteristics

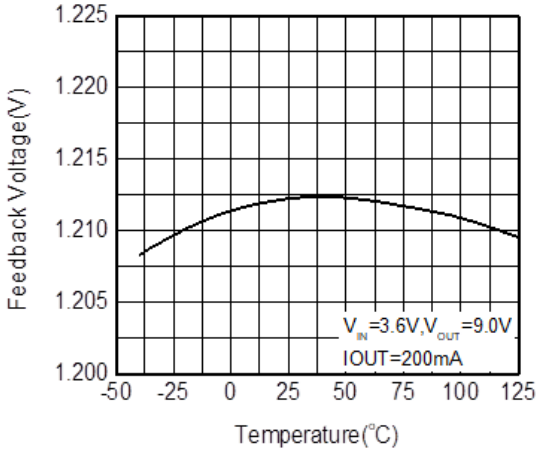
(Ta=25°C,V_{IN}=3.6V,V_{EN}=3.6V,V_{OUT} =9V,L1=1.8uH,C_{IN}=22uF,C_{OUT}=3×22μF,C4=0.1uF,C3=2.2uF,unless otherwise noted)

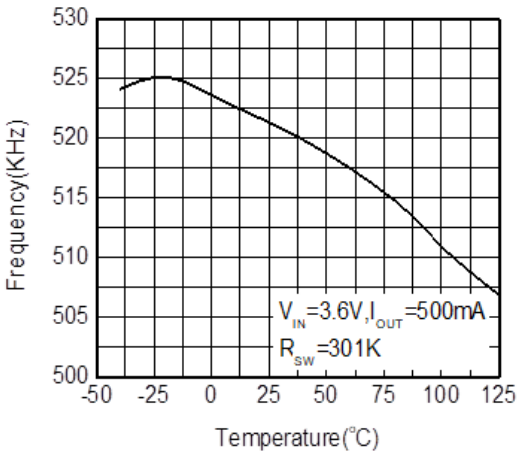












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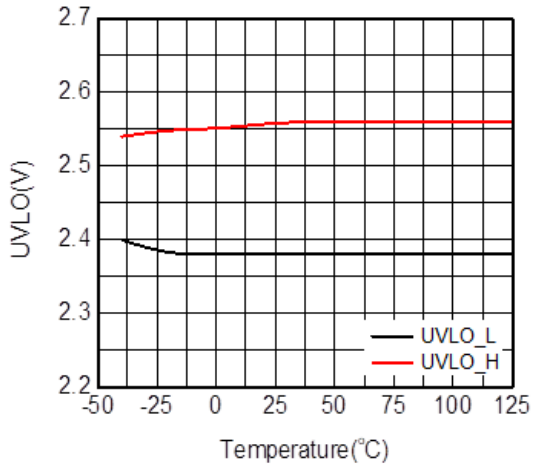
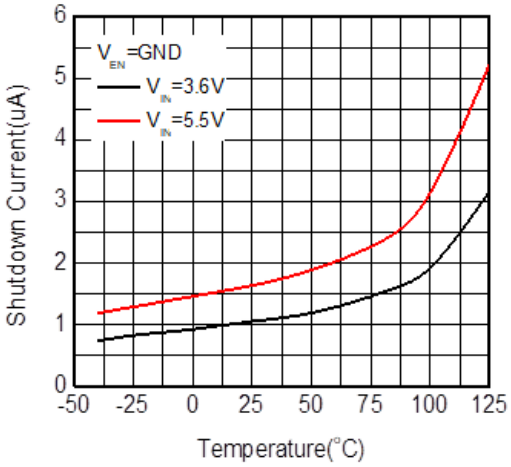
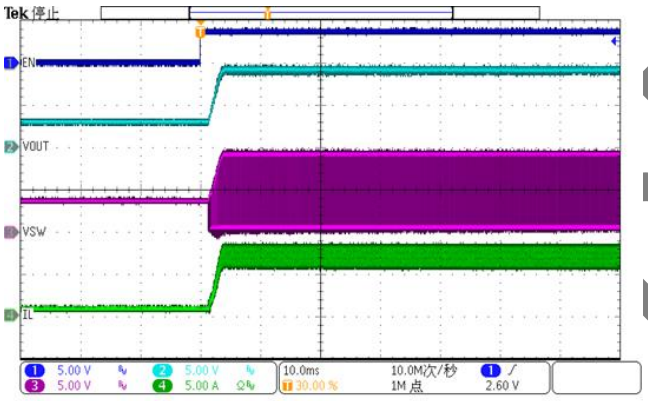
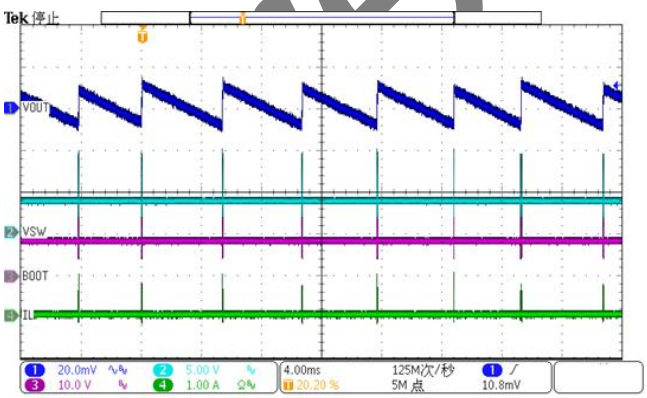






Startup, VIN =3.6V, VOUT = 9V, IOUT =2A



Ripple, VIN =3.6V, VOUT = 9V, IOUT =0A

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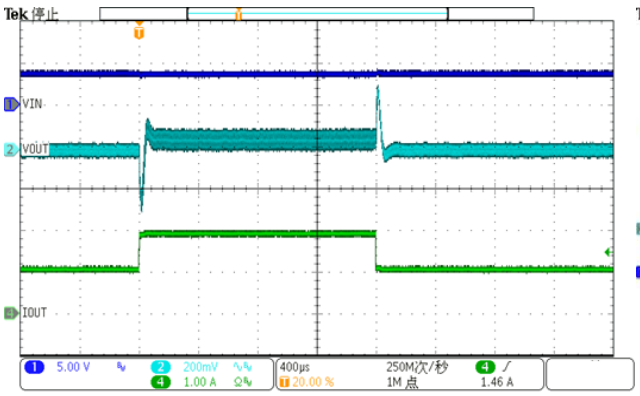
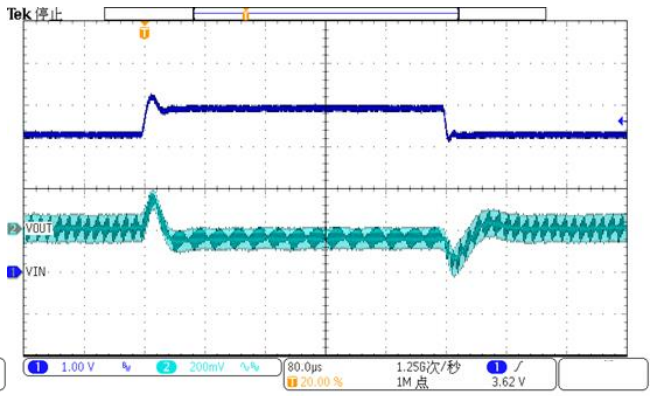


Load Transient, VIN =3.6V, VOUT = 9V, IOUT =1A to 2A



Line Transient, VIN =3.3V to 4V, VOUT = 9V, IOUT =2A

Operation Informations

The WD31089Q is a synchronous boost converter that is capable to output continuous power more than 18W from input of a single cell Lithium-ion battery or two-cell Lithium-ion batteries in series. The WD31089Q operates at a quasi-constant frequency with constant off peak current mode control scheme at moderate to heavy load currents, which provides excellent line and load transient response. At light load condition, the WD31089Q operates in PFM mode to improve efficiency. The external loop compensation brings flexibility to use different inductors and output capacitors. The device implements cycle-by-cycle current limit to protect the device from overload conditions during boost mode.

Undervoltage Lockout (UVLO)

An under-voltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the typical UVLO threshold of 2.5 V. A hysteresis of 200 mV is added so that the device cannot be enabled again until the input voltage goes up to 2.7 V. This function is implemented in order to prevent malfunctioning of the device when the input voltage is between 2.5 V and 2.7 V.

Enable and Disable

When the input voltage is above maximal UVLO rising threshold of 2.7 V and the EN pin is pulled above the high threshold, the WD31089Q is enabled. When the EN pin is pulled below the low threshold, the WD31089Q goes into shutdown mode. The device stops switching in the shutdown mode and consumes less than 1µA current (typ.). Because of the body diode of the high side rectifier FET, the input voltage goes through the body diode and appears at the V_{OUT} pin at the shutdown mode.

Soft Start

The WD31089Q implements the soft start function to reduce the inrush current during startup. The WD31089Q begins soft start when the EN pin is pulled to logic high voltage. The soft start time is typically 4ms.

Adjustable Switching Frequency

The WD31089Q features a wide adjustable switching frequency ranging from 200kHz to 2.2MHz. The switching frequency is set by a resistor connected between the FSW pin and the SW pin of the WD31089Q. Do not leave the FSW pin open. Use Equation 1 to calculate the resistor value required for a desired frequency.

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$$R_{FREQ} = \frac{4\times\left(\frac{1}{f_{SW}} - t_{DELAY}\times\frac{V_{OUT}}{V_{IN}}\right)}{C_{FREQ}} \quad (1)$$

where

• R_{FREQ} is the resistance connected between the FSW pin and the SW pin.

• C_{FREQ} = 24 pF

• f_{SW} is the desired switching frequency.

• t_{DELAY} = 86 ns

• V_{IN} is the input voltage.

• V_{OUT} is the output voltage.

Adjustable Peak Current Limit

To avoid an accidental large peak current, an internal cycle-by-cycle current limit is adopted. The low-side switch turns off immediately as long as the peak switch current touches the limit. The peak inductor current can be set by selecting the correct external resistor value correlating with the required current limit. Use Equation 2 to calculate the correct resistor value for the WD31089Q.

$$I_{LIM} = \frac{1030000}{R_{ILIM}} \quad (2)$$

where

• R_{ILIM} is the resistance connected between the ILIM pin and ground.

• I_{LIM} is the switch peak current limit.

For a typical current limit of 8 A, the resistor value is 127 kΩ for the WD31089Q.

Overvoltage Protection

If the output voltage at the V_{OUT} pin is detected above over-voltage protection threshold of 13.2 V (typical value), the WD31089Q stops switching immediately until the voltage at the V_{OUT} pin drops the hysteresis voltage lower than the output over-voltage protection threshold. This function prevents over-voltage on the output and secures the circuits connected to the output from excessive overvoltage.

Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically, the thermal shutdown happens at the junction temperature of 155°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 130°C, then the device starts switching again.

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Application Informations

Setting Output Voltage

The output voltage is set by an external resistor divider (R1, R2). Typically, a minimum current of 10μA flowing through the feedback divider gives good accuracy and noise covering. A resistor of less than 120kΩ is typically selected for low-side resistor R2.

When the output voltage is regulated, the typical voltage at the FB pin is V_{REF}. Thus the value of R1 is calculated as:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (3)$$

Inductor Selection

Because the selection of the inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. Three most important specifications to the performance of the inductor are the inductor value, DC resistance, and saturation current.

The WD31089Q is designed to work with inductor values between 0.47μH and 10μH. A 0.47μH inductor is typically available in a smaller or lower-profile package, while a 10μH inductor produces lower inductor current ripple. If the boost output current is limited by the peak current protection of the IC, using a 10μH inductor can maximize the controller's output current capability. Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0A current depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow Equation 4 to Equation 4 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, TI recommends using the minimum switching frequency, the inductor value with –30% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in Equation 4.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (4)$$

where

- V_{OUT} is the output voltage of the boost regulator.
- I_{OUT} is the output current of the boost regulator.
- V_{IN} is the input voltage of the boost regulator.
- η is the power conversion efficiency.

Calculate the inductor current peak-to-peak ripple as in Equation 5.

$$I_{PP} = \frac{1}{L \times (\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}) \times f_{SW}} \quad (5)$$

where

- I_{PP} is the inductor peak-to-peak ripple.
- L is the inductance value.
- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Therefore, the peak current, I_{Lpeak}, seen by the inductor is calculated with Equation 6.

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2} \quad (6)$$

Set the current limit of the WD31089Q higher than the peak current I_{Lpeak}. Then select the inductor with saturation current higher than the setting current limit.

Boost converter efficiency is dependent on the resistance of its current path, the switching loss associated with the switching MOSFETs, and the inductor's core loss. The WD31089Q has optimized the internal switch resistance. However, the overall efficiency is affected significantly by the inductor's DC resistance (DCR), and the core loss. Core loss is related to the core material and different inductors have different core loss. For a

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certain inductor, larger current ripple generates higher DCR and core loss. Usually, the datasheet of components don't provide the core loss information. If needed, consult the inductor vendor for detailed information. Generally, we would recommend an inductor with lower DCR and core loss. However, there is a tradeoff among the inductor's inductance, DCR and ESR resistance, and its footprint. Furthermore, shielded inductors typically have higher DCR than unshielded inductors. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation.

Input Capacitor Selection

For good input voltage filtering, ceramic capacitors with low-ESR Will recommended. The VIN pin is the power supply for the WD31089Q. A 0.1μF ceramic bypass capacitor is recommended as close as possible to the V_{IN} pin of the WD31089Q. The V_{CC} pin is the output of the internal LDO. A ceramic capacitor of more than 1.0 μF is required at the V_{CC} pin to get a stable operation of the LDO. For the power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 10μF input capacitance is sufficient for most applications.

Output Capacitor Selection

For small output voltage ripple, low-ESR output capacitor such as ceramic capacitor is recommended. Typically, three 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Take care when evaluating a capacitor's derating under DC bias. The DC bias can significantly reduce the effective capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the following equations to calculate the minimum required effective capacitance C_O:

$$V_{ripple\_dis} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_O} \quad (7)$$

$$V_{ripple\_ESR} = I_{Lpesk} \times R_{ESR} \quad (8)$$

where

- V_{ripple_dis} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter's switching frequency.
- R_{ESR} is the ESR of the output capacitors.

PC Board Layout Considerations

The device is designed to operate from an input voltage supply range between 2.7V to 12V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47μF.

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability and noise problems. To maximize efficiency, switching rise time and fall time are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs to

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be close to the VIN pin and GND pin in order to reduce the input supply current ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the V_{OUT} pin, but also to the GND pin to reduce the overshoot at the SW pin and V_{OUT} pin.

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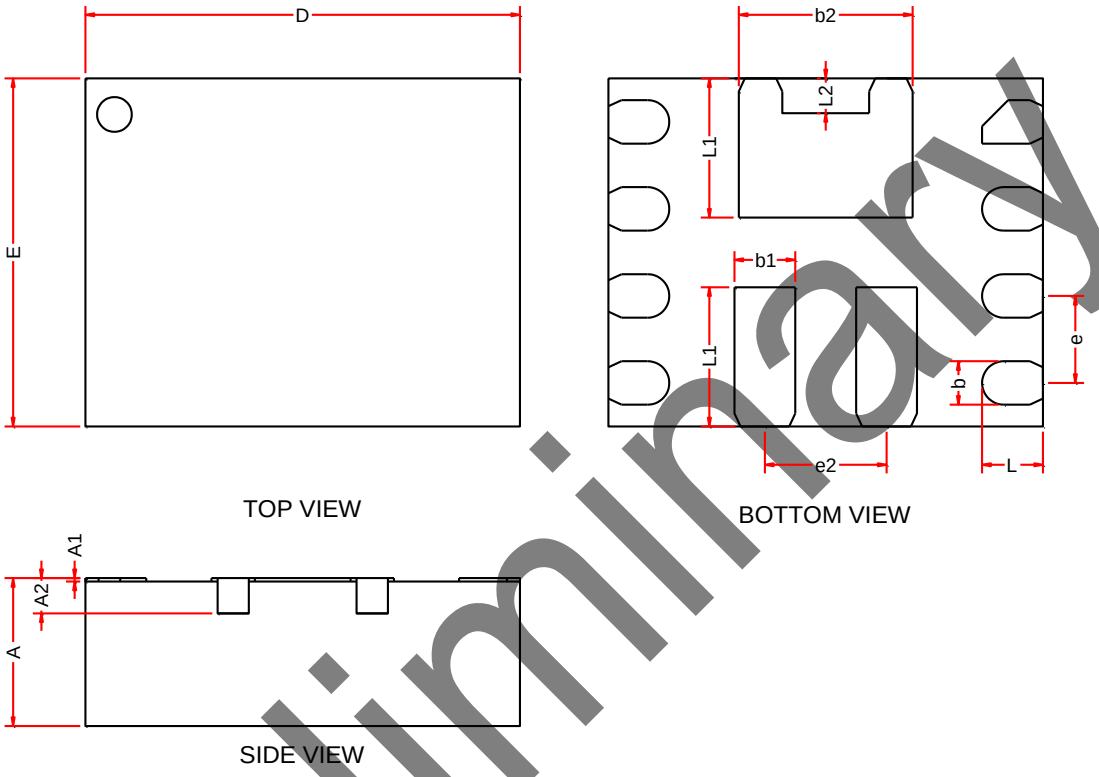
PACKAGE OUTLINE DIMENSIONS

QFN2520-12L



Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.80	0.85	0.90
A1	--	0.02	0.05
A2	0.203REF		
D	2.5BSC		
E	2.00BSC		
b	0.20	0.25	0.30
b1	0.30	0.35	0.45
b2	0.95	1.00	1.05
L	0.25	0.35	0.45
L1	0.75	0.80	0.85
L2	0.20REF		
e	0.50BSC		
e2	0.70BSC		

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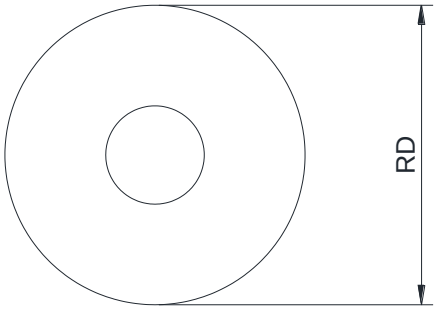
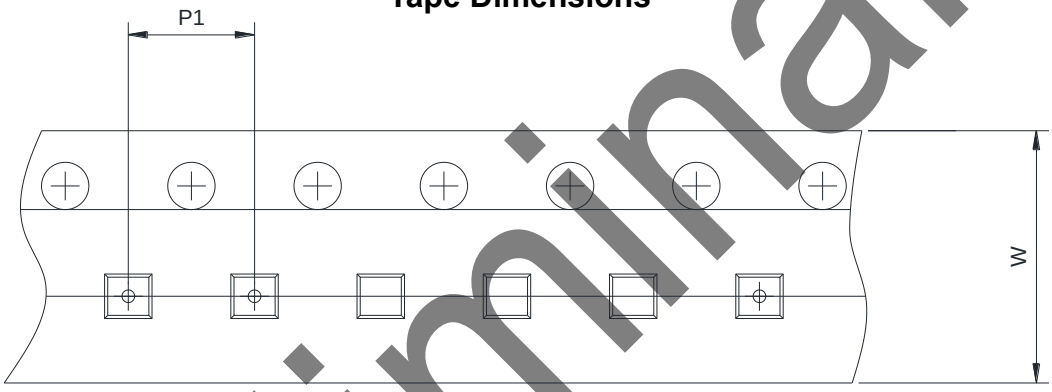
TAPE AND REEL INFORMATION

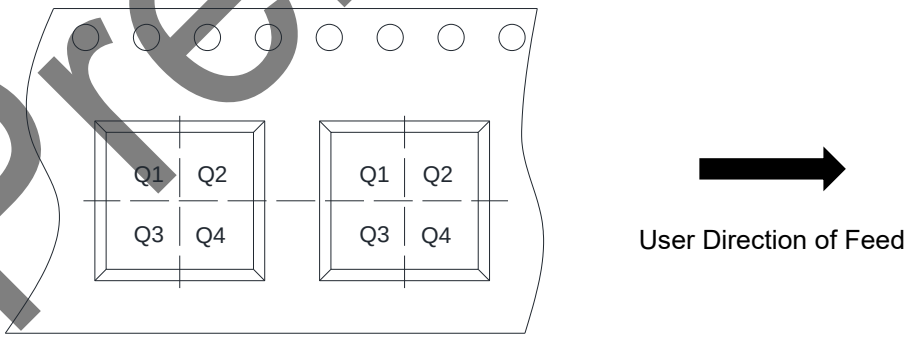
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm		
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☐ Q1	☑ Q2	☐ Q3	☐ Q4

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