WD1050C08

6MHz, 750mA Miniature, Adjustable, Step-Down DC-DC Converter for RF Power Amplifiers

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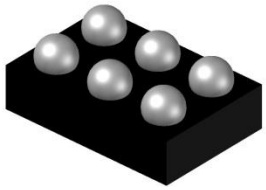
Descriptions

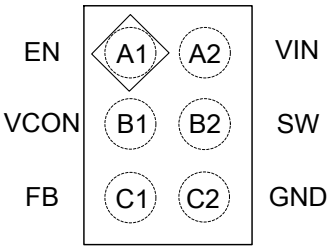
The WD1050C08 is a DC-DC step-down converter specialized for powering RF power amplifiers (PAs) from a single Lithium-Ion battery; And it can be used to power other hand-held Radio devices. By using an input voltage from 2.7V to 5.5V, it can generate an adjustable output voltage from 0.6V to 3.4V by the communication from one analog pin VCON.

The WD1050C08 offers three modes of operation. In PWM mode the device operates at a fixed frequency of 6MHz (typ.), which minimizes EMI when driving medium-to-heavy loads and which allows use of tiny surface-mount components, an inductor and two ceramic capacitors. At light load, the device switches into PSM (power saving mode) mode automatically and operates with reduced quiescent current and switching frequency to extend battery life. The device is off in shutdown mode and reduces battery consumption to 100nA (typ.).

The WD1050C08 is available in CSP-6L package. Standard products are Pb-Free and Halogen-Free.

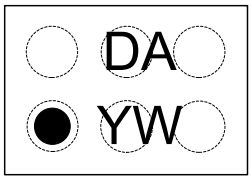


CSP-6L



CSP-6L

Pin configuration (Top view)



CSP-6L

DA = Device code
Y = Year code
W = Week code

Marking

Features

- 6MHz (typ.) PWM Switching Frequency
- Operates from a Single Li-Ion Cell (2.7V to 5.5V)
- One-pin (VCON) adjusts Output Voltage (0.6V to 3.4V)
- 750 mA Maximum Load Capability
- High Efficiency (95% typ. at 3.6VIN, 3.3VOUT at 300 mA)
- Adaptive PSM/PWM mode change depending on load condition
- Over-Current Protection
- Over-Thermal Protection
- Soft Start Function

Order information

Device	Package	Shipping
WD1050C08-6/TR	CSP-6L	3000/Reel&Tape

Applications

- Battery-Powered 3G/4G Power Amplifiers
- Hand-Held Radios
- RF PC Cards
- Battery-Powered RF Devices

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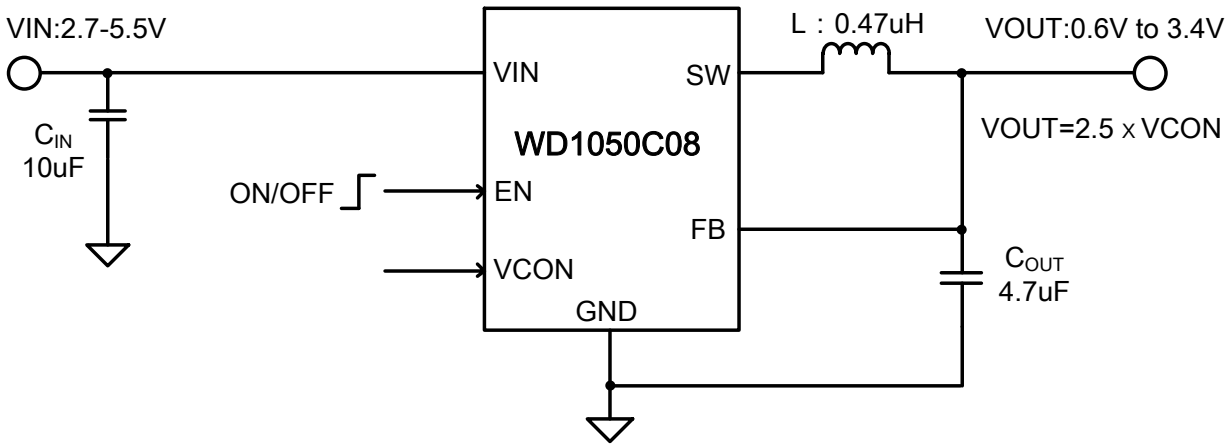
Typical Applications



Pin Descriptions

Symbol	Pin Number	Descriptions
EN	A1	Enable Input. Set this digital input high for normal operation. For shutdown, set low. Do not leave EN pin floating.
VCON	B1	Voltage Control Analog input. VCON controls VOUT in PWM mode. Do not leave VCON pin floating. VOUT = 2.5 x VCON.
FB	C1	Feedback Analog Input. Connect to the output at the output inductor.
GND	C2	Ground
SW	B2	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the maximum Switch Peak Current Limit specification of the WD1050C08.
VIN	A2	Power supply input. Connect to the input filter capacitor (Typical Application Circuit).

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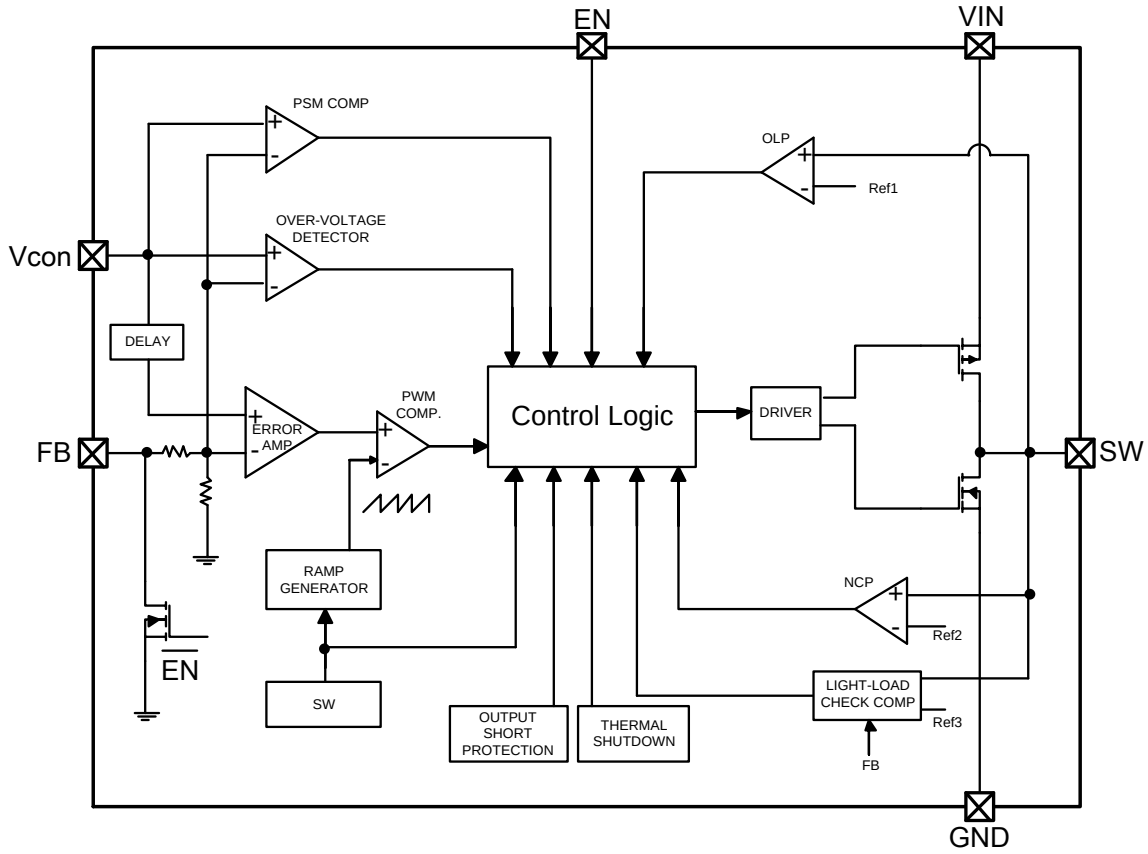
Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
VIN pin voltage range	V_{IN}	-0.2～+6.0	V
EN、FB、VCON、SW pin voltage range	-	（GND-0.2）～（V_{IN} +0.2）w/6.0	V
Continuous Power Dissipation (Note 1)	P_D	Internally Limited	-
Maximum Junction Temperature	T_{J-MAX}	+150	°C
Junction-to-Ambient Thermal Resistance (Note 2)	$R_{\theta JA}$	85	°C/W
Maximum Lead temperature(Soldering, 10s)	T_L	+260	°C
Operating ambient temperature	T_A	-40 ~ 85	°C
Storage temperature	T_{stg}	-65 ~ +150	°C
ESD Classification	HBM	±3000	V
	CDM	±2000	V

These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Note 1: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typ.).

Note 2: Junction-to-ambient thermal resistance ($R_{\theta JA}$) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7.

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Electrical Characteristics

The parameters in the electrical characteristics table are tested under open loop conditions at VIN=3.6V unless otherwise specified. For performance over the input voltage range and closed-loop results, refer to the datasheet curves.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Voltage Range	V_{IN}		2.7		5.5	V
Feedback Voltage at minimum setting	$V_{FB,MIN}$	PWM mode, VCON=0.24V	0.51	0.6	0.69	V
Feedback Voltage at maximum setting	$V_{FB,MAX}$	PWM mode, VCON=1.36V, V_{IN} =3.9V	3.332	3.4	3.468	V
Shutdown Supply Current	I_{SHDN}	V_{EN} = V_{SW} = VCON=0V		0.1	2	μA
PSM mode Quiescent Current	I_Q_PSM	PSM mode, No switching VCON=0.8V, V_{FB} = 2.05V		50	70	μA
$R_{DS(ON)}$ of P-Channel FET	R_{PFET}	V_{IN}=V_{GS}=3.6V, I_{SW}=200mA		160	250	mΩ
$R_{DS(ON)}$ of N-Channel FET	R_{NFET}	V_{IN}=V_{GS}=3.6V, I_{SW}=-200mA		130	220	
PFET switch Peak Current Limit	I_{LIM}	V_{IN}=4V, V_{OUT}=2V	1300	1500	1700	mA
Switching Frequency	F_{OSC}		5	6	7	MHz
VCON to V_{OUT} gain	Gain	0.24V ≤ VCON ≤1.36V		2.5		V/V
EN Rising Threshold	V_{EN}-H		1.4			V
EN falling Threshold	V_{EN}-L				0.4	V

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System Characteristics

The following spec table entries are guaranteed by design providing the component values in the Typical Application Circuit are used. These parameters are not verified by production testing. Min and Max values apply over the following conditions (V_{IN}=2.7V to 5.5V, L = 0.47µH, C_{IN} = 10 µF, 6.3V, 0603 (1608), C_{OUT} = 4.7 µF, 6.3V, 0603 (1608), Ta=25°C, unless otherwise noted).

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
VCON pin leakage current	I_{CON}	VCON=1.0V			±1	µA
Maximum output current capability	I_{OUT}	2.7V ≤ V_{IN} ≤5.5V, 0.24V ≤ VCON ≤1.36V	750			mA
V_{OUT} step rise time from 0.6V to 3.4V(to reach 3.26V)	T_{CONTR}	VIN=3.6V,VCON=0.24V to 1.36V,VCON T_R=1uS,R_{LOAD}=10Ω			25	µS
V_{OUT} step fall time from 3.4V to 0.6V(to reach 0.74V)		VIN=3.6V,VCON=1.36V to 0.24V,VCON T_F=1uS,R_{LOAD}=10Ω			25	
Maximum Duty Cycle	D	100% allowed during dropout	100			%
Linearity in control range 0.24V to 1.36V	Δ_{LINE}	Monotronic in nature	-3		+3	%
			-50		+50	mV
Turn-on Time(time for output to reach 95% final value after Enable low-to-high transition)	T_{ON}	EN=Low-To-High V_{IN}=4.2V,V_{OUT}=3.4V I_{OUT} = <1mA ,C_{OUT}=4.7µF			50	µS
Efficiency	η	V_{IN}=3.6V, V_{OUT}=0.8V I_{OUT} = 10mA, PSM mode		65		%
		V_{IN}=3.6V, V_{OUT}=1.8V I_{OUT} = 200mA,PWM mode		87		
		V_{IN}=3.9V, V_{OUT}=3.3V I_{OUT} = 500mA,PWM mode		92		
Line transient response	$LINE_{TR}$	V_{IN}=3.6V to 4.2V,T_R=T_F=10µS, I_{OUT} = 100mA, V_{OUT}=0.8V		50		mV_{PK}
Load transient response	$LOAD_{TR}$	V_{IN}=3.1V/3.6V/4.5V, V_{OUT}=0.8V I_{OUT} = 50mA to 150mA, T_R=T_F=0.1µS		50		

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Typical Characteristics

(Ta=25°C, V_{IN}=V_{EN}=3.6V , L=0.47µH, C_{IN}=10µF, C_{OUT}=4.7µF, unless otherwise noted)

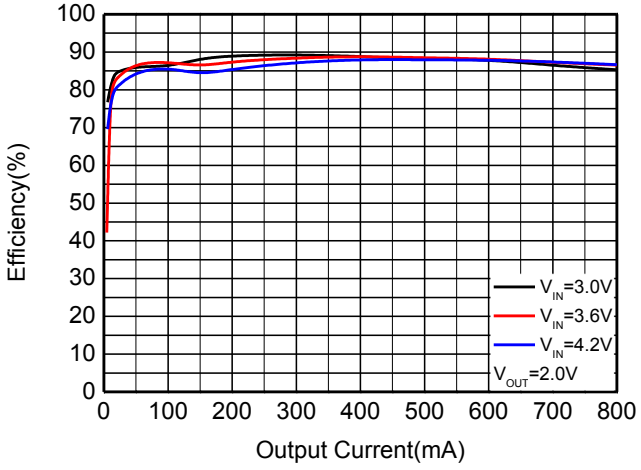

Figure 1.

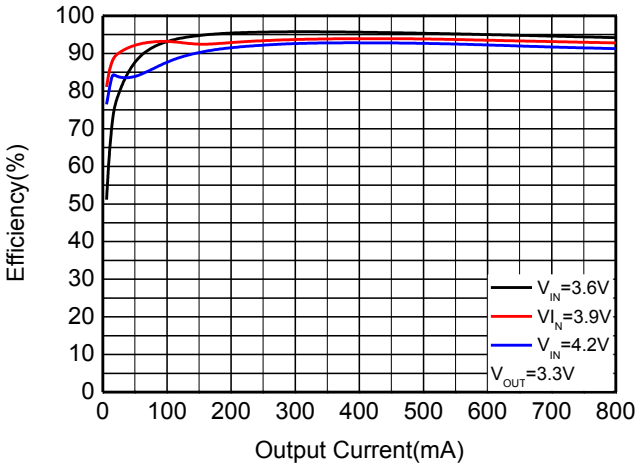

Figure 2.

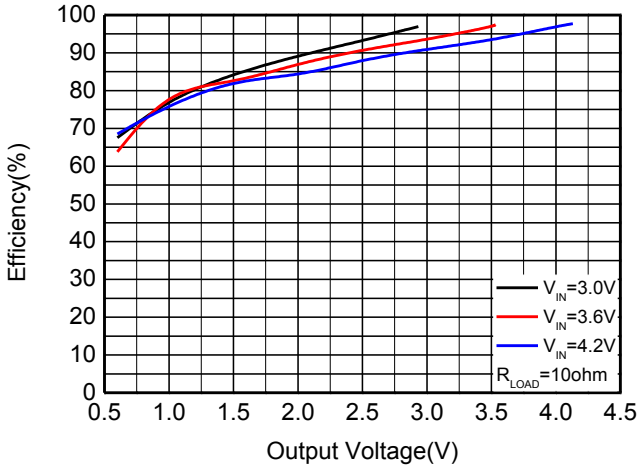

Figure 3.

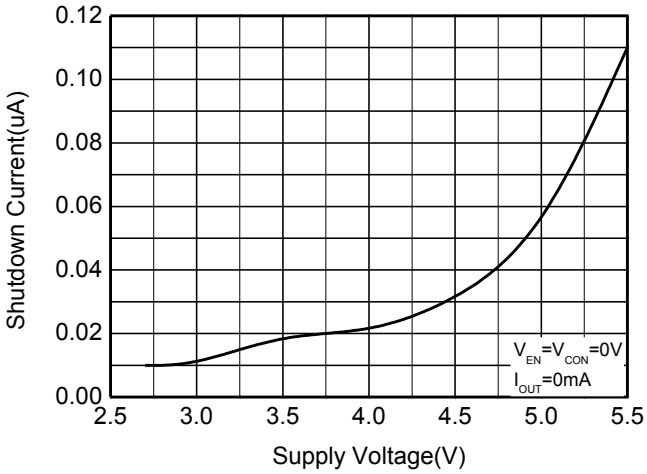

Figure 4.

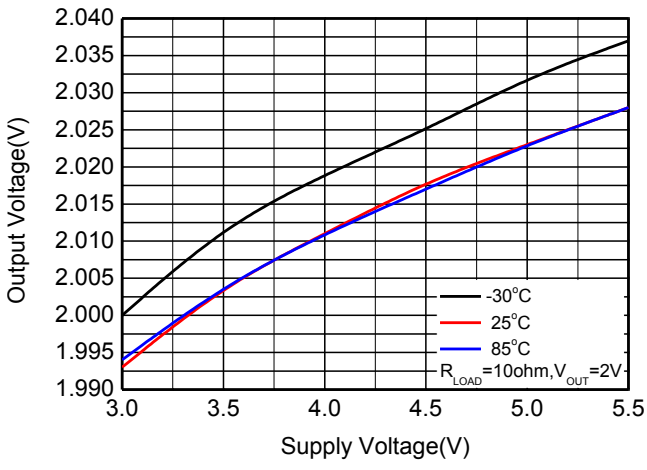

Figure 5.

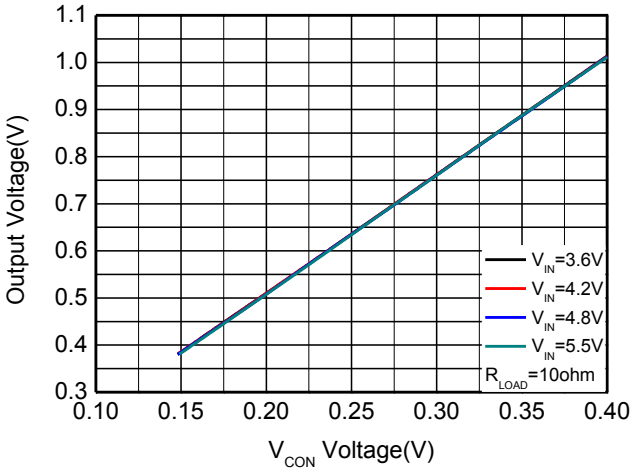

Figure 6.

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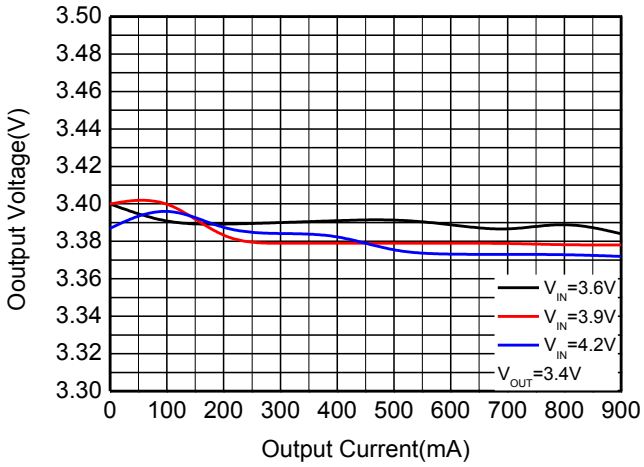


Figure 7.

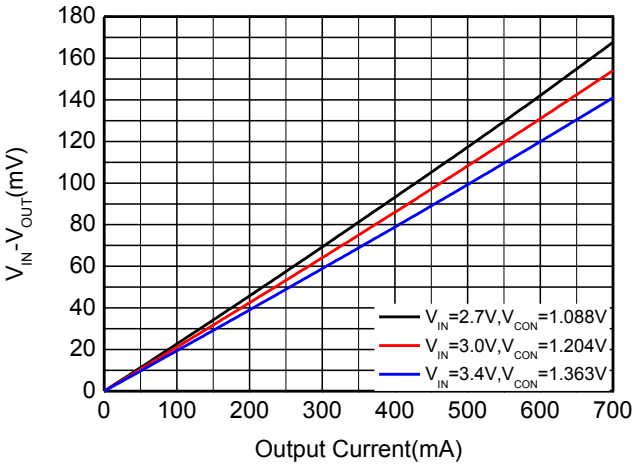


Figure 8.

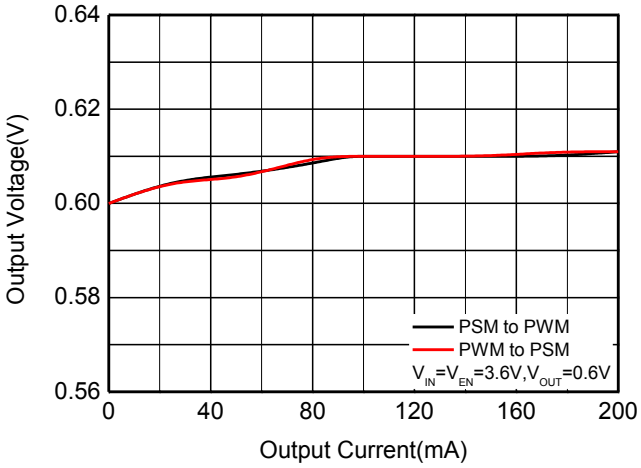


Figure 9.

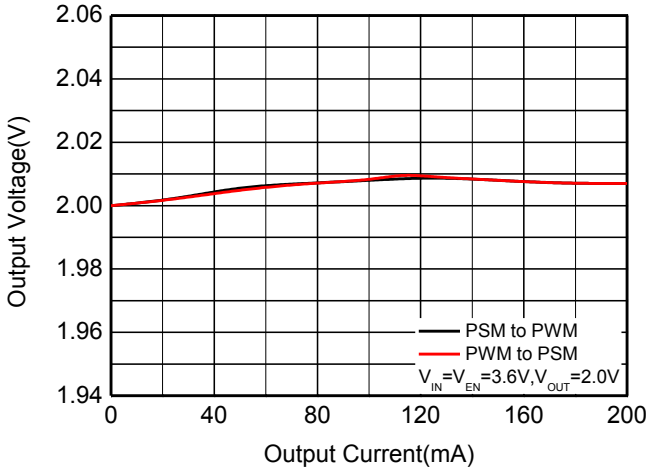


Figure 10.

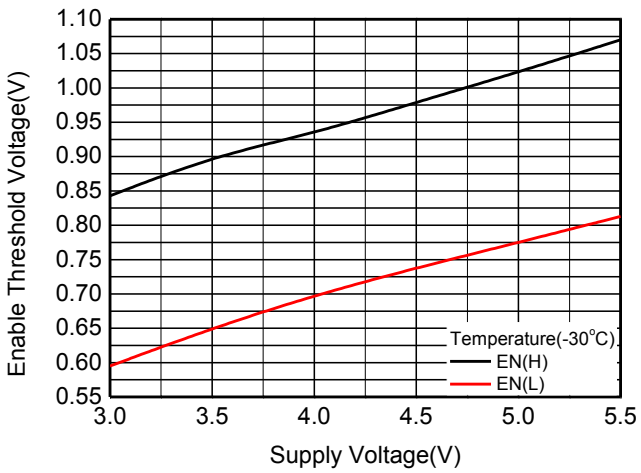
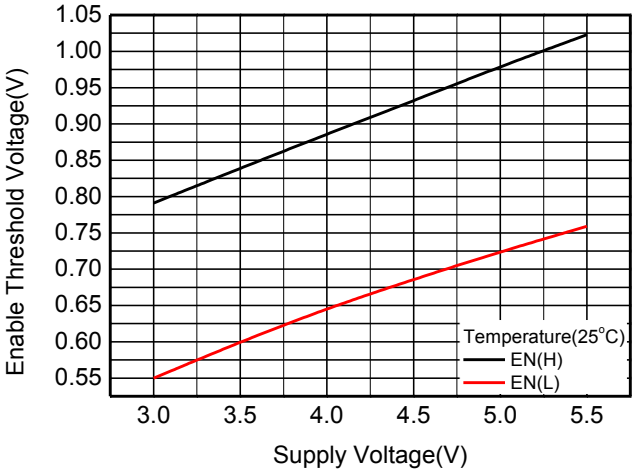


Figure 11



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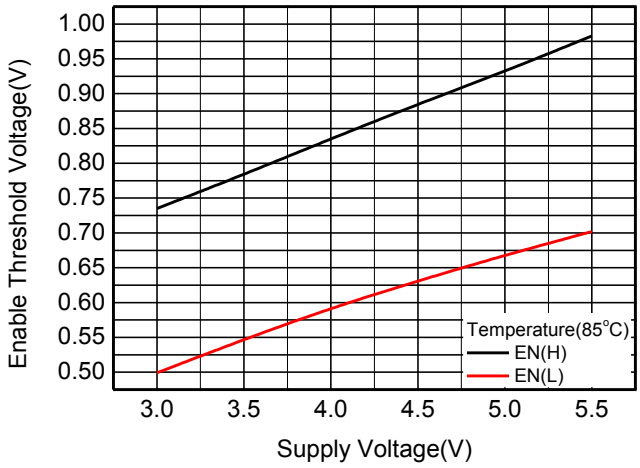


Figure 13.

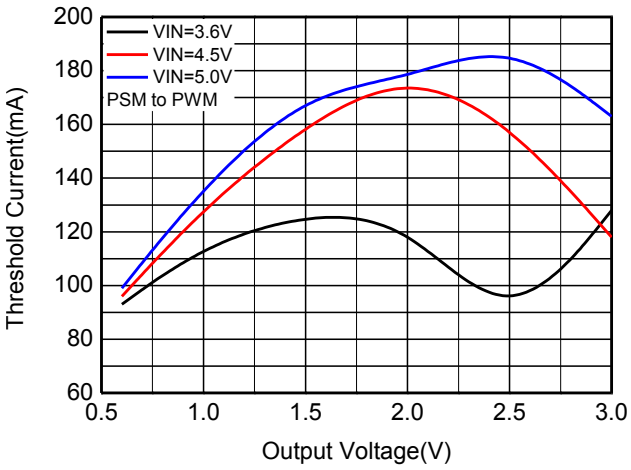


Figure 14.

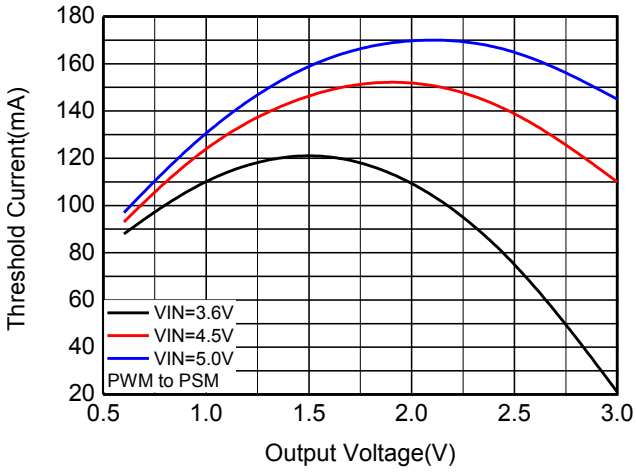
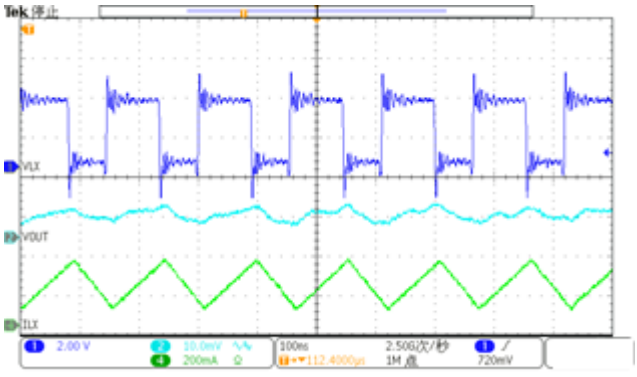


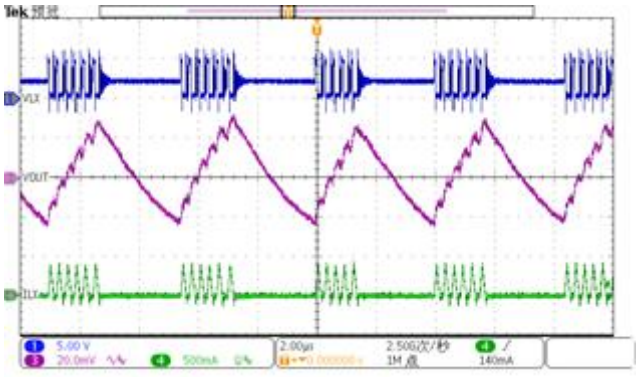
Figure 15.



Output Voltage Ripple in PWM Mode

VIN=EN=3.6V, VO=2V, IOUT=200mA

Figure 16



Output Voltage Ripple in PSM Mode

VIN=EN=5V, VO=2V, IOUT=50mA

Figure 17

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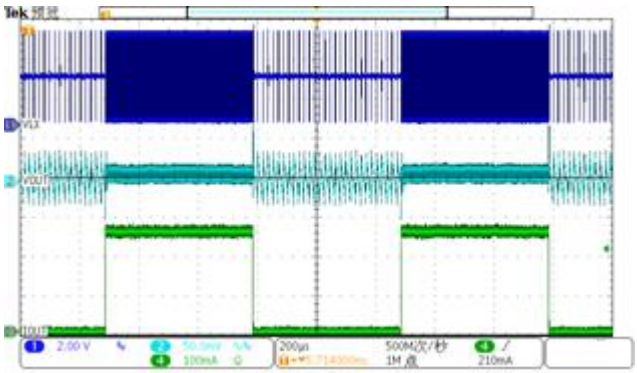
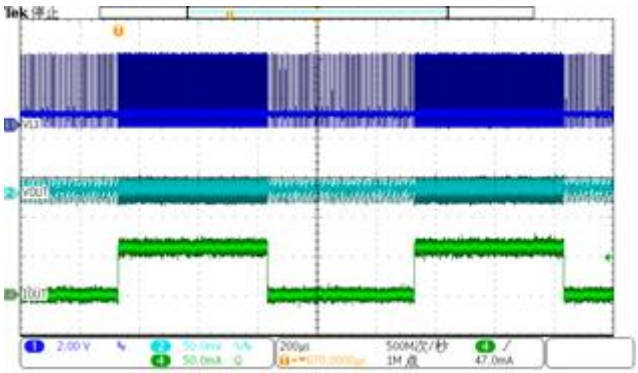


Load Transient Response

VIN=EN=5V, VO=2.5V, IO=10mA-250mA

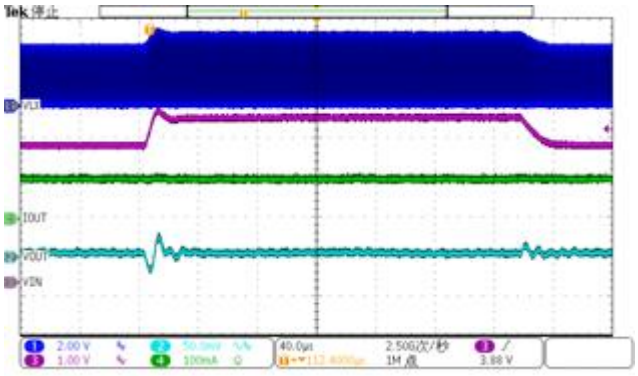
Figure 18.



Load Transient Response

VIN=EN=4V, VO=0.6V,IO=10mA-60mA

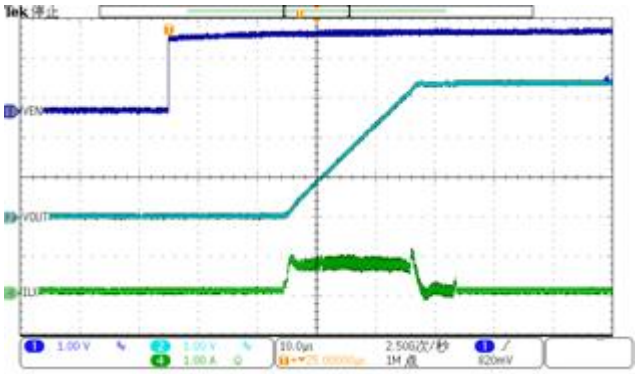
Figure 19.



Line Transient Response

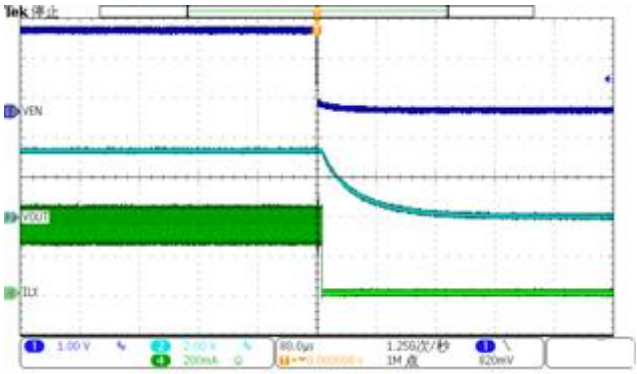
VIN=3.6V-4.2V, VO=0.8V, R_{LOAD}=8Ω

Figure 20.



VIN=4.2V, VO=3.4V，EN=2V,RLOAD=3.3kΩ, EN On

Figure 21.



VIN=4.2V, VO=3.4V，EN=2V , RLOAD=10Ω, EN Off

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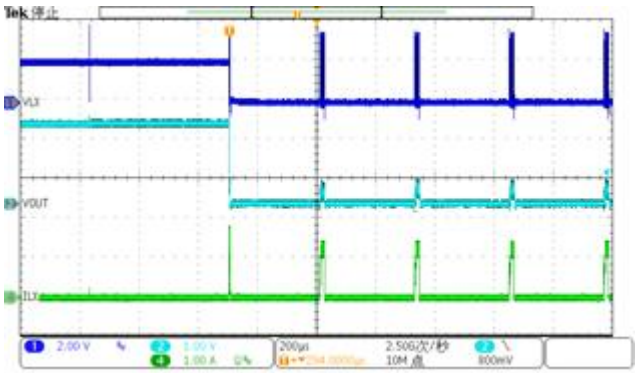

Output Short to Ground，VIN=EN=3.6V, VO=2V

Figure 23.

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Operation Informations

Device Information

The WD1050C08 is a simple, step-down DC-DC converter optimized for powering RF power amplifiers (PAs) in mobile phones, portable communicators, and similar battery-powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency over a wide range of power levels from a single Li-Ion battery cell. It is based on a voltage-mode buck architecture, with synchronous rectification for high efficiency. It is designed for a maximum load capability of 750 mA in PWM mode. Maximum load range may vary from this depending on input voltage, output voltage and the inductor chosen.

There are three modes of operation depending on the current required: PWM (Pulse Width Modulation), PSM, and shutdown. The WD1050C08 operates in PWM mode at higher load current conditions. Lighter loads cause the device to automatically switch into PSM mode. Shutdown mode turns the device off and reduces battery consumption to 0.1 µA (typ.).

DC PWM mode output voltage precision is ±2% for 3.4VOUT. Efficiency is typically around 93% (typ.) for a 500mA load with 3.3V output, 3.9V input. The output voltage is dynamically programmable from 0.6V to 3.4V by adjusting the voltage on the control pin (VCON) without the need for external feedback resistors. This ensures longer battery life by being able to change the PA supply voltage dynamically depending on its transmitting power.

Additional features include current overload protection and thermal overload shutdown.

The WD1050C08 is constructed using a chip-scale 6-bump CSP-6L package. This package offers the smallest possible size for space-critical applications, such as cell phones, where board area is an important design consideration. Use of a high switching frequency (6MHz, typ.) reduces the size of external components. As shown in the Typical Application Circuit, only three external power components are required for implementation. Use of a CSP-6L package requires special design considerations for implementation. Its fine-bump pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subject to high-intensity ambient red or infrared light. Also, the system controller should set EN low during power-up and other low supply voltage conditions.

Circuit Operation

Referring to the Typical Application Circuit and the BLOCK DIAGRAM, the WD1050C08 operates as follows. During the first part of each switching cycle, the control block in the WD1050C08 turns on the internal top-side PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of around (VIN - VOUT) / L, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the bottom-side NFET synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope around VOUT / L. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at SW to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

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PWM Mode Operation

While in PWM mode operation, the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced. At the beginning of each ON-time cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by a comparator turning off the NFET and turning on the PFET.

PSM Mode Operation

At very light loads, the WD1050C08 enters PSM mode operation with reduced switching frequency and supply current to maintain high efficiency. During PSM mode operation, the WD1050C08 positions the output voltage slightly higher than the normal output voltage during PWM mode operation, allowing additional headroom for voltage drop during a load transient from light to heavy load.

Shutdown Mode

Setting the EN digital pin low (<0.4V) places the WD1050C08 in Shutdown mode (0.1 µA typ.). During shutdown, the PFET switch, the NFET synchronous rectifier, reference voltage source, control and bias circuitry of the WD1050C08 are turned off. Setting EN high (>1.2V) enables normal operation. EN should be set low to turn off the WD1050C08 during power-up and undervoltage conditions when the power supply is less than the 2.7V minimum operating voltage. The WD1050C08 has an UVLO (Under Voltage Lock Out) comparator to turn the power device off in the case the input voltage or battery voltage is too low. The typical UVLO threshold is around 2.4V for lock and 2.5V for release.

Internal Synchronization Rectification

While in PWM mode, the WD1050C08 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

With medium and heavy loads, the NFET synchronous rectifier is turned on during the inductor current down slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

Current Limiting

The current limit feature allows the WD1050C08 to protect itself and external components during overload conditions. In PWM mode, the cycle-by-cycle current limit is 1450 mA (typ.). If an excessive load pulls the output voltage down to less than 0.3V (typ.), the converter enters hiccup, thereby preventing excess current and thermal stress.

Dynamically Adjustable Output Voltage

The WD1050C08 features dynamically adjustable output voltage to eliminate the need for external feedback resistors. The output can be set from 0.6V to 3.4V by changing the voltage on the analog VCON pin. This feature is useful in PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life.

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Thermal Overload Protection

The WD1050C08 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 155°C, the device inhibits operation. Both the PFET and the NFET are turned off. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

Soft Start

The WD1050C08 has a soft-start circuit that limits in-rush current during startup. During startup the switch current limit is increased in steps. Soft start is activated if EN goes from low to high after V_{IN} reaches 2.7V.

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Application Informations

Output Voltage Setting

The WD1050C08 features a pin-controlled adjustable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.6V to 3.4V by setting the voltage on the VCON pin, as in the following formula:

$$V_{OUT} = 2.5 \times VCON \quad (1)$$

When VCON is between 0.24V and 1.36V, the output voltage will follow proportionally by 2.5 times of VCON.

If VCON is less than 0.24V (V_{OUT} = 0.6V), the output voltage may be regulated. Refer to datasheet curve (Low VCON Voltage vs. Output Voltage) for details. This curve exhibits the characteristics of a typical part, and the performance cannot be guaranteed as there could be a part-to-part variation for output voltages less than 0.6V.

Inductor Selection

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings over the ambient temperature of application should be requested from manufacturer.

Minimum value of inductance to guarantee good performance is 0.3 µH at bias current (ILIM (typ.)) over the ambient temperature range. Shielded inductors radiate less noise and should be preferred. There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as:

$$I_{SAT} > I_{OUT\_MAX} + I_{RIPPLE}$$

Where

$$I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: average-to-peak inductor current
- I_{OUT_MAX}: maximum load current (750 mA)
- V_{IN}: maximum input voltage in application
- L: minimum inductor value including worst-case tolerances (30% drop can be considered for Method 1)
- F: minimum switching frequency (5 MHz)
- V_{OUT}: output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that can handle the maximum current limit of 1600 mA.

The inductor's resistance should be less than around 0.1Ω for good efficiency.

Capacitor Selection

The WD1050C08 is designed for use with ceramic capacitors for its input and output filters. Use a 10 µF ceramic capacitor for input and a 4.7 µF ceramic capacitor for output. They should maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitors type such as X5R, X7R, and B are recommended for both filters. They provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. For CIN, use of an 0805 (2012) size may also be considered if there is room on the system board.

The input filter capacitor supplies AC current drawn by the PFET switch of the WD1050C08 in

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the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes, and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

PC Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the CSP-6L package and board pads — poor solder joints can result in erratic or degraded performance. Good layout for the WD1050C08 can be implemented by following a few simple design rules, as illustrated in below Figure.

1. Place the WD1050C08, inductor, and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching current and act as antennae. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the VIN and GND pads.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the WD1050C08 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the WD1050C08 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. Connect the ground pads of the WD1050C08 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the WD1050C08 by giving it a low impedance ground connection.
4. Use side traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
5. Route noise sensitive traces such as the voltage feedback path away from noisy traces between the power components. The output voltage feedback point should be taken approximately 1.5 nH away from the output capacitor. The feedback trace also should be routed opposite to noise components. The voltage feedback trace must remain close to the WD1050C08 circuit and should be routed directly from FB to VOUT at the inductor and should be routed opposite to noise components. This allows fast feedback and reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.

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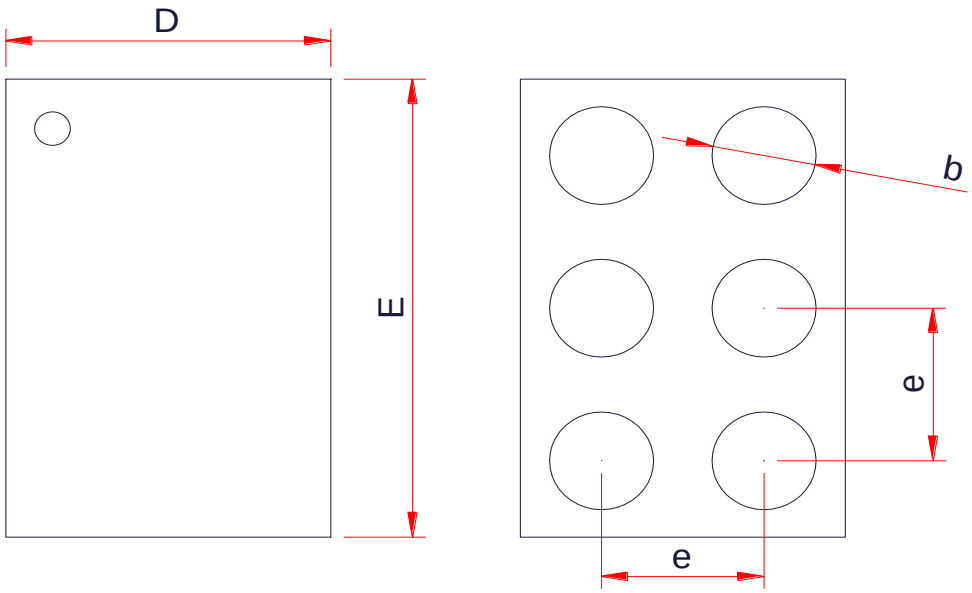
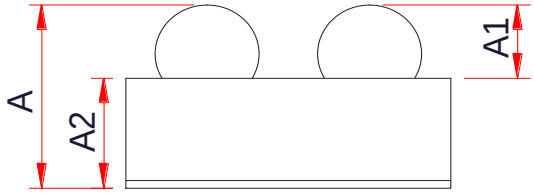
PACKAGE OUTLINE DIMENSIONS

CSP-6L



TOP VIEW BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.53	0.57	0.60
A1	0.16	0.19	0.21
A2	0.36	0.38	0.40
D	0.94	0.97	1.00
E	1.44	1.47	1.50
e	0.50 Typ.		
b	0.21	0.23	0.25

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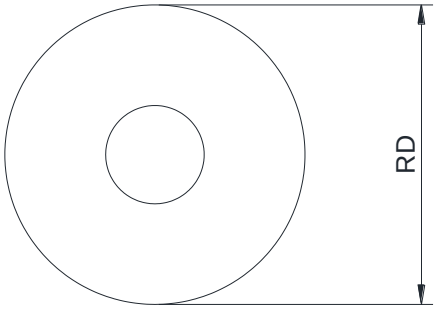
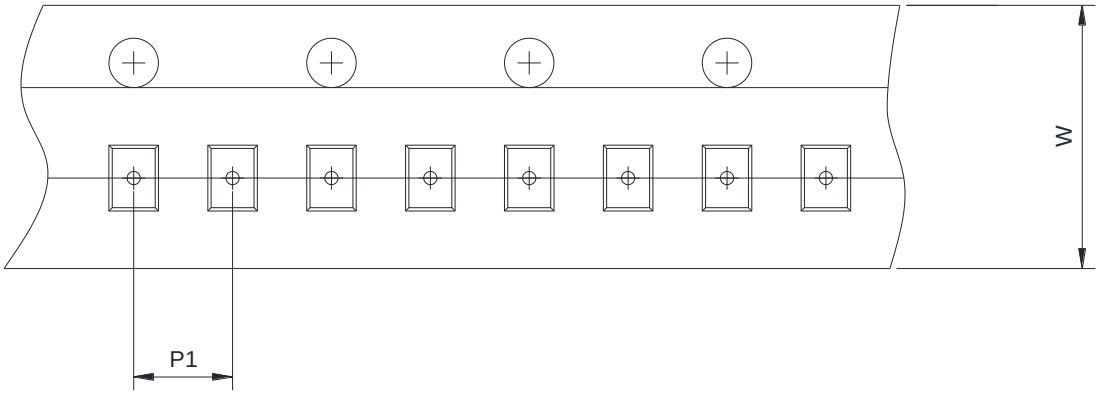
TAPE AND REEL INFORMATION

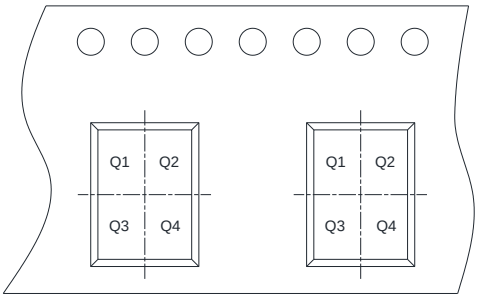
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



User Direction of Feed

RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4

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