

# WS4666D

6A, 19m $\Omega$ , Dual Channel Load Switch with Quick Output Discharge and Adjustable Rise Time

### **Descriptions**

The WS4666D is a dual channel load switch that provides configurable rise time to minimize inrush current. The device contains two N-channel MOSFETs that can operate over an input voltage range of 0.6V to 5.5V and can support a maximum continuous current of 6A. The switch is controlled by an on/off input (ON), which is capable of interfacing directly with low-voltage control signals. In the WS4666D, a 54 $\Omega$  on-chip load resistor is added for quick output discharge when the switch is turned off.

The WS4666D is available in a small, space-saving DFN3x2-14L package.Standard product is Pb-free and Halogen-free.

### Features

- Integrated Dual Channel Load Switch
- Input Voltage Range: 0.6V to 5.5V
- Ultra-Low On Resistance ( $R_{ON}$ )  $R_{ON} = 19m\Omega$  at  $V_{IN} = 5V$  ( $V_{BIAS} = 5V$ )
- 6 A Maximum Continuous Switch Current
- Low Control Input Threshold Enables Use of 1.2V, 1.8V, 2.5V and 3.3V Logic
- Configurable Rise Time
- Quick Output Discharge (QOD)
- DFN3x2-14L Package
- ESD Performance Tested per JESD 22 2kV HBM and 1kV CDM

# Applications

- Ultrabook ™
- Notebooks/Netbooks
- Tablet PC
- Consumer Electronics
- Set-top Boxes/Residential Gateways
- Telecom Systems





DFN3X2-14L



#### Pin configuration (Top view)



For detail order information, please see page 2.

#### **Order Information**

For detail order information, please see page 2.

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# **Order Information**

Ordering No.	Continuous Current	Rise Time	Enable	Output Shutdown Resistor	Package	Operating Temperature	Marking	Shipping
WS4666DAB	64	Adjustable	Active	540	DFN3x2	40, 40500	4666	3000/Reel
-14/TR	-14/TR	Aujustable	Adjustable High		-14L	-40~105°C	ABYW	&Tape

#### **Marking Information**

- 4666 = Device code
  - \*\* = Special code
  - Y = Year code
  - W = Week code

Marking

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# **Typical Application**



### **Pin Description**

PIN No.	Symbol	I/O	Description
			Switch1 input. Input bypass capacitor recommended for minimizing $V_{\ensuremath{IN}}$
1,2	VINI		dip.
3	ON1	Ι	Active high switch1 control input. Do not leave floating.
4 VBIAS I Bias voltage. Power supply to for this pin is 2.7V to 5.5V.			Bias voltage. Power supply to the device. Recommended voltage range
		I	for this pin is 2.7V to 5.5V.
5	ON2	I	Active high switch2 control input. Do not leave floating.
		1	Switch2 input. Input bypass capacitor recommended for minimizing $V_{\ensuremath{\mathbb{N}}}$
0,7	VIINZ		dip.
8,9	VOUT2	0	Switch2 output.
10	CT2	0	Switch2 slew rate control. Can be left floating.
11	GND		Ground
12	CT1	0	Switch1 slew rate control. Can be left floating.
13,14	VOUT1	0	Switch1 output.
	Thermal PAD		Thermal PAD. Tie to GND

### **Block Diagram**



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#### **Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit	
V <sub>IN1,2</sub>	Input voltage range		-0.3 ~ 6	V
V <sub>OUT1,2</sub>	Output voltage range		-0.3 ~ 6	V
VBIAS	Bias voltage range		-0.3 ~ 6	V
V <sub>ON1,2</sub>	ON pin voltage range	-0.3 ~ 6	V	
IMAX	Maximum continuous swit	6	A	
I <sub>PLS</sub>	Maximum pulsed switch c	8	A	
TA	Operating free-air tempera	-40 ~ 105	°C	
TJ	Maximum junction temper	ature	125	°C
T <sub>STG</sub>	Storage temperature rang	e	-40 ~ 125	°C
T <sub>LEAD</sub>	Maximum lead temperatu	260	°C	
ESD	Electrostatic discharge	Human-Body Model (HBM)	±2000	V
ESD	protection Charged-Device Model (CDM		±1000	v

#### **Thermal Information**

Symbol	Parameter	WS4666D DFN3*2-14L	Unit
R <sub>0JA</sub>	Junction-to-Ambient thermal resistance <sup>*1</sup>	73	°C/W
R <sub>0JC(top)</sub>	Junction-to-Case (Top) Thermal Resistance	62	°C/W
R <sub>0JC(bottom)</sub>	Junction-to-Case (Bottom) Thermal Resistance	17	°C/W
R <sub>0JB</sub>	Junction-to-Board Thermal Resistance	41	°C/W

\*1:Surface mounted on FR-4 Board using 2 oz, 1 square inch Cu area, PCB board size 1.5\*1.5 square inches

### **Recommended Operating Ratings**

Symbol	Parameter	Min	Max	Unit	
VIN1,2	Input voltage range	0.6	VBIAS	V	
VBIAS	Bias voltage range			5.5	V
V <sub>ON1,2</sub>	ON voltage range	0	5.5	V	
V <sub>OUT1,2</sub>	Output voltage range			V <sub>IN</sub>	V
VIH	High-level input voltage, ON	V <sub>BIAS</sub> =2.7V to 5.5V	1.2	5.5	V
VIL	Low-level input voltage, ON	0	0.4	V	
C <sub>IN1,2</sub>	Input capacitor				μF

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### **Electrical Characteristics**

 $V_{BIAS}$ =5.0V, Cin=1µF, T<sub>A</sub>=25°C, unless otherwise noted.

Parameter	Symbol	Test Con	ditions	Min	Тур	Max	Unit
V <sub>BIAS</sub> Quiescent Current		I <sub>OUT1</sub> =I <sub>OUT2</sub> =0m/	۹,		40	66	
(Both Channels)	1	$V_{IN1,2} = V_{ON1,2} = \xi$	5.0V		49	00	μΑ
V <sub>BIAS</sub> Quiescent Current	IQ,VBIAS	I <sub>OUT1</sub> =I <sub>OUT2</sub> =0m/	A, V <sub>ON2</sub> = 0V		20	56	
(Single Channel)		$V_{IN1,2} = V_{ON1} = 5.$	0V		39	50	μΑ
V <sub>BIAS</sub> Shutdown Current	I <sub>SD,VBIAS</sub>	V <sub>ON1,2</sub> = 0V , V <sub>OU</sub>	<sub>T1,2</sub> = 0V		0.3	1	μA
			VIN = 5.0V		0.08	1	
V <sub>IN</sub> Shutdown Current	les	$V_{ON} = 0V$ ,	VIN = 3.3V		0.025	0.4	
(Per Channel)	ISD,VIN	V <sub>OUT</sub> = 0V	VIN = 1.8V		0.015	0.3	μΑ
			VIN = 0.6V		0.01	0.15	
ON Pin Input Leakage Current	I <sub>ON</sub>	V <sub>ON</sub> = 5.5V				0.1	μA
			$V_{IN} = 5.0V$		19	28	
			V <sub>IN</sub> = 3.3V		19	28	
ON-state Resistance	R <sub>ON</sub>	Ι <sub>ΟUT</sub> = -200mA,	V <sub>IN</sub> = 1.8V		19	28	- m0
(Per Channel)		$V_{BIAS} = 5.0V$	V <sub>IN</sub> = 1.2V		19	28	
			V <sub>IN</sub> = 1.05V		19	28	
			$V_{IN} = 0.6V$		19	28	
ON Pin Hysteresis	V <sub>ON,HYS</sub>	V <sub>IN</sub> =5.0V			90		mV
Output Pull-down	D				E A		0
Resistance	<b>r</b> pd	$v_{\rm IN} = v_{\rm OUT} = 5.0V, v_{\rm ON} = 0V$			54	00	12
Thermal Shutdown	T <sub>SD</sub>	Junction tempera	ature rising		160		°C
Thermal Shutdown Hysteresis	T <sub>SD,HYS</sub>	Junction tempera	ature falling		25		°C

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# **Electrical Characteristics (Continued)**

 $V_{BIAS}$ =2.7V, Cin=1µF, T<sub>A</sub>=25°C, unless otherwise noted.

Parameter	Symbol	Test Con	ditions	Min	Тур	Max	Unit
V <sub>BIAS</sub> Quiescent Current		I <sub>OUT1</sub> =I <sub>OUT2</sub> =0m/	I <sub>OUT1</sub> =I <sub>OUT2</sub> =0mA,		27	40	ΠΑ
(Both Channels)		$V_{IN1,2} = V_{ON1,2} = 2$	2.5V		21	40	μπ
V <sub>BIAS</sub> Quiescent Current	IQ,VBIAS	I <sub>OUT1</sub> =I <sub>OUT2</sub> =0m/	A, V <sub>ON2</sub> = 0V		24	35	114
(Single Channel)		$V_{IN1,2} = V_{ON1} = 2.$	5V		24	- 55	μΛ
VBIAS Shutdown Current	I <sub>SD,VBIAS</sub>	V <sub>ON1,2</sub> = 0V , V <sub>OU</sub>	<sub>JT1,2</sub> = 0V		0.1	1	μA
			V <sub>IN</sub> = 2.5V		0.02	0.36	
VIN Shutdown Current	les	$V_{ON} = 0V$ ,	V <sub>IN</sub> = 1.8V		0.015	0.3	
(Per Channel)	ISD,VIN	V <sub>OUT</sub> = 0V	V <sub>IN</sub> = 1.05V		0.015	0.25	μΑ
			V <sub>IN</sub> = 0.6V		0.01	0.15	
ON Pin Input Leakage Current	I <sub>ON</sub>	V <sub>ON</sub> = 5.5V				0.1	μA
			V <sub>IN</sub> = 2.5V		20	28	- mΩ
			V <sub>IN</sub> = 1.8V		20	28	
ON-state Resistance	Ron	I <sub>оит</sub> = -200mA,	V <sub>IN</sub> = 1.5V		20	28	
(Per Channel)		$V_{BIAS} = 2.7V$	V <sub>IN</sub> = 1.2V		20	28	
			V <sub>IN</sub> = 1.05V		20	28	
			V <sub>IN</sub> = 0.6V		19	28	
ON Pin Hysteresis	V <sub>ON,HYS</sub>	V <sub>IN</sub> =2.5V			50		mV
Output Pull-down	<b>D</b>		$\lambda = 0 \lambda$			00	0
Resistance	RPD	$v_{\rm IN} = v_{\rm OUT} = 2.5 V, V_{\rm ON} = 0 V$			51	80	Ω
Thermal Shutdown	T <sub>SD</sub>	Junction temperature rising			160		°C
Thermal Shutdown Hysteresis	T <sub>SD,HYS</sub>	Junction tempera	ature falling		25		°C

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# **Switching Characteristics Measurement Information**



# **Switching Characteristics**

	Parameter	Test Conditions	Min Typ Max	Unit				
V <sub>IN</sub> = V <sub>ON</sub> = V <sub>BIAS</sub> = 5V, T <sub>A</sub> = 25 °C (unless otherwise noted)								
t <sub>ON</sub>	Turn-on time		1800					
t <sub>OFF</sub>	Turn-off time		0.85					
t <sub>R</sub>	V <sub>OUT</sub> rise time	$R_L = 10\Omega$ , $C_L = 0.1 \mu$ F, $C_T = 1000 \mu$ F	2300	μs				
t⊨	V <sub>OUT</sub> fall time		1.75					
t <sub>D</sub>	ON delay time		800					
V <sub>IN</sub> = 0	$0.6V, V_{ON} = V_{BIAS} = 5$	V, T <sub>A</sub> = 25 °C (unless otherwise noted)						
ton	Turn-on time		725					
toff	Turn-off time		1.15					
t <sub>R</sub>	$V_{\text{OUT}}$ rise time	R∟ = 10Ω, C∟ = 0.1uF, C⊤ = 1000pF	360	μs				
t⊢	V <sub>OUT</sub> fall time		1.6					
t <sub>D</sub>	ON delay time		540					
V <sub>IN</sub> = 2	2.5V, V <sub>ON</sub> = 5V, V <sub>BIAS</sub>	= 2.7V, $T_A$ = 25 °C (unless otherwise noted	)	1				
t <sub>ON</sub>	Turn-on time		1750					
toff	Turn-off time		1.05					
t <sub>R</sub>	V <sub>OUT</sub> rise time	R∟ = 10Ω, C∟ = 0.1uF, C⊤ = 1000pF	2065	μs				
t⊢	V <sub>OUT</sub> fall time		2					
t <sub>D</sub>	ON delay time		820					
V <sub>IN</sub> = 0	0.6V, V <sub>ON</sub> = 5V, V <sub>BIAS</sub>	= 2.7V, T <sub>A</sub> = 25 °C (unless otherwise noted	)					
t <sub>ON</sub>	Turn-on time		1050					
t <sub>OFF</sub>	Turn-off time		1.2					
t <sub>R</sub>	$V_{\text{OUT}}$ rise time	R∟ = 10Ω, C∟ = 0.1uF, C⊤ = 1000pF	560	μs				
t⊦	Vout fall time		1.3					
t <sub>D</sub>	ON delay time		740					

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# Typical DC Characteristics



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# **Typical DC Characteristics (Continued)**



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# **Typical DC Characteristics (Continued)**





2.0

1.8

Bias Voltage (V) VON Hysteresis VS. Bias Voltage

4.0

4.5

5.0

5.5

6.0

3.0

2.5

3.5

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# **Typical AC Characteristics**



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# **Typical AC Characteristics (Continued)**



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### **Working Waveforms**



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#### **Detailed Description**

#### Overview

The WS4666D device is a dual channel,  $19m\Omega$  load switch in a DFN3x2-14L package.Each channel can support a maximum continuous current of 6 A and is controlled by an on and off GPIO-compatible input. To reduce the voltage drop in high current rails, the device implements N-channel MOSFETs. The device has a configurable slew rate for applications that require a specific rise-time.

The device prevents downstream circuits from pulling high standby current from the supply by limiting the leakage current of the device when it is disabled. The integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

#### Adjustable Rise Time

A capacitor to GND on the CT pin sets the slew rate. To ensure desired performance, a capacitor with a minimum voltage rating of 25 V must be used on either CT pins. This equation accounts for 10% to 90% measurement on VOUT and does not apply for CT < 100 pF.

Use Table 1 to determine rise times for when CT = 0 pF.

#### $SR = 0.45 \times C_T + 30$

where

- SR is the slew rate (in µs/V)
- CT is the capacitance value on the CT pin (in pF)
- The units for the constant 30 are  $\mu$ s/V. The units for the constant 0.45 are  $\mu$ s/(V × pF).

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device. Rise times shown in Table 1 are only valid for the power-up sequence where VIN and VBIAS are already in steady state condition before the ON pin is asserted high.

CT(pF)	RISE TIME(us) 10%-90% ,CL=0.1μF,CIN=1μF,RL=10Ω,V <sub>BIAS</sub> =5V							
	VIN=5V	VIN=3.3V	VIN=1.8V	VIN=1.5V	VIN=1.2V	VIN=1.05V	VIN=0.6V	
0	247	180	110	100	89	84	63	
220	645	417	263	234	205	190	138	
470	1056	671	421	373	325	298	209	
1000	1949	1231	763	672	577	527	364	
2200	4032	2523	1545	1351	1150	1049	711	
4700	9165	5580	3332	2915	2468	2238	1567	
10000	19810	12040	7179	6257	5314	4785	3213	

#### Table 1. Rise Time tR vs CT Capacitor

\*1:Typical Values at 25  $^\circ$ C with a 25V X7R 10% Ceramic Capacitor on CT.

#### ON and OFF Control

The ON pin controls the state of the switch. ON is active high and has a 1.2 V ON pin enable threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

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#### Input Capacitor (C<sub>IN</sub>) (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1 $\mu$ F ceramic capacitor, C<sub>IN</sub>, placed close to the pins, is usually sufficient. Higher values of C<sub>IN</sub> can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor (C<sub>L</sub>) to avoid excessive voltage drop.

#### Output Capacitor (C<sub>L</sub>) (Optional)

Because of the integrated body diode in the NMOS switch, a CIN greater than CL is highly recommended. A CL greater than CIN can cause VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A CIN to CL ratio of 10 to 1 is recommended for minimizing VIN dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more VIN dip upon turn-on because of inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time.

#### **Quick-Output Discharge**

When the switch is disabled, an internal discharge resistance is connected between VOUT and GND to remove the remaining charge from the output. This resistance has a typical value of 230  $\Omega$  and prevents the output from floating while the switch is disabled. For best results, it is recommended that the device gets disabled before VBIAS falls below the minimum recommended voltage.

#### **Thermal Shutdown**

Thermal shutdown protects the part from internally or externally generated excessive temperatures. When the device temperature triggers TSD (typical 160°C), the switch is turned off. The switch automatically turns on again if the temperature of the die drops 20 degrees below the TSD threshold.

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# PACKAGE OUTLINE DIMENSIONS



<u>Cumbal</u>	Dimensions in Millimeters				
Зутьої	Min.	Тур.	Max.		
A	0.70	0.75	0.80		
A1	0.02 0.05				
A2	0.203REF				
D	3BSC				
E		2BSC			
E1	0.75	0.80	0.85		
D1	2.45	2.50	2.55		
b	0.15 0.20 0.25				
e	0.4BSC				
L	0.30 0.35 0.40				

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## TAPE AND REEL INFORMATION

#### **Reel Dimensions**





# **Quadrant Assignments For PIN1 Orientation In Tape**





User Direction of Feed

RD	Reel Dimension	🗹 7inch	🔲 13inch		
W	Overall width of the carrier tape	🗹 8mm	🔲 12mm		
P1	Pitch between successive cavity centers	🔲 2mm	🗹 4mm	🔲 8mm	
Pin1	Pin1 Quadrant	🔽 Q1	🗖 Q2	🗖 Q3	🗖 Q4

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