WD1020/WD1021

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Ultra-Low Quiescent Current Buck Converter

Descriptions

The WD1020 and the WD1021 are efficient synchronous step-down converters with ultra-low quiescent current of typical 360 nA. The devices provide high efficiency at light load down to 10 µA. The input voltage ranges from 2.2 V to 5.5 V. The output voltage is programmable between 1.2 V and 3.3 V. The WD1020 delivers output current up to 600 mA, peak to 1.2 A. The WD1021 delivers output current 400 mA, peak to 0.8 A.

The peak current operation with internal compensation allows the transient response to be optimized over a wide range of loads and output capacitors.

The WD1020 and the WD1021 are available in CSP-8L packages. Standard products are Pb-free and Halogen-free.

Features

- Input voltage range: 2.2 V to 5.5 V
- 1 MHz frequency
- Ultra-low 360 nA Iq, up to 94% efficiency
- Light load PFM operation
- Output discharge
- 8-Level programmable output voltage
  - WD1020 1.2 V to 3.3 V
  - WD1021 0.7 V to 3.1 V
- Output current
  - WD1020 600 mA, peak to 1.2 A
  - WD1021 400 mA, peak to 0.8 A
- Automatic transition to 100% duty cycle

Applications

- Wearable devices, internet of things
- Hand-held devices, portable information
- Battery powered equipment

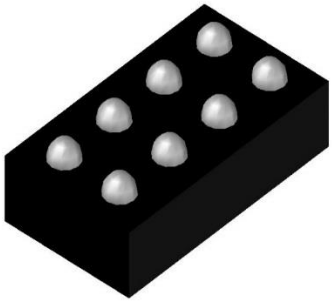
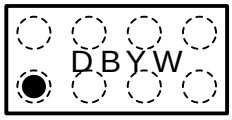


Figure 1 CSP-8L (Bottom View)

WD1020

DA = Device code
Y = Year code
W = Week code

WD1021



DB = Device code
Y = Year code
W = Week code

Figure 2 Markings (Top View)

Order Information

Table 1

Device	Package	Shipping
WD1020C-8/TR	CSP-8L	3000/Reel &Tape
WD1021C-8/TR	CSP-8L	3000/Reel &Tape

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Pin Information

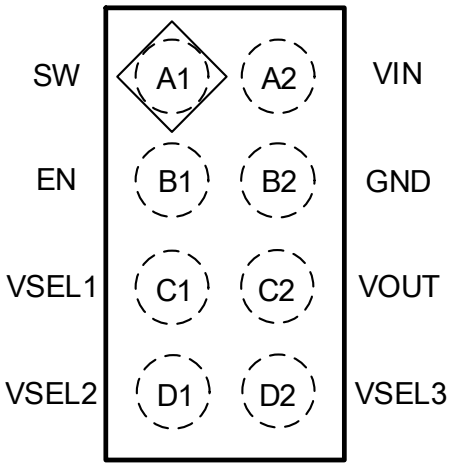

Figure 3 Pin Information

Table 2

Pin	Symbol	Description
A1	SW	The pin is the connection between two build-in switches in the chip. The pin needs to be connected to the external inductor with the shortest path.
A2	VIN	Power supply input. Connect to the input filter capacitor (Typical Application Circuit).
B1	EN	Chip enable input pin. High-level voltage enables the device while low-level voltage turns off the device. The pin must be terminated.
B2	GND	Device ground pin. The pin needs to be connected to input and output capacitors with the shortest path.
C1	VSEL1	Output voltage selection pin. The pin must be terminated.
C2	VOUT	Output voltage feedback pin. The pin needs to be connected close to the output capacitor terminal for voltage regulation.
D1	VSEL2	Output voltage selection pin. The pin must be terminated.
D2	VSEL3	Output voltage selection pin. The pin must be terminated.

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Block Diagram

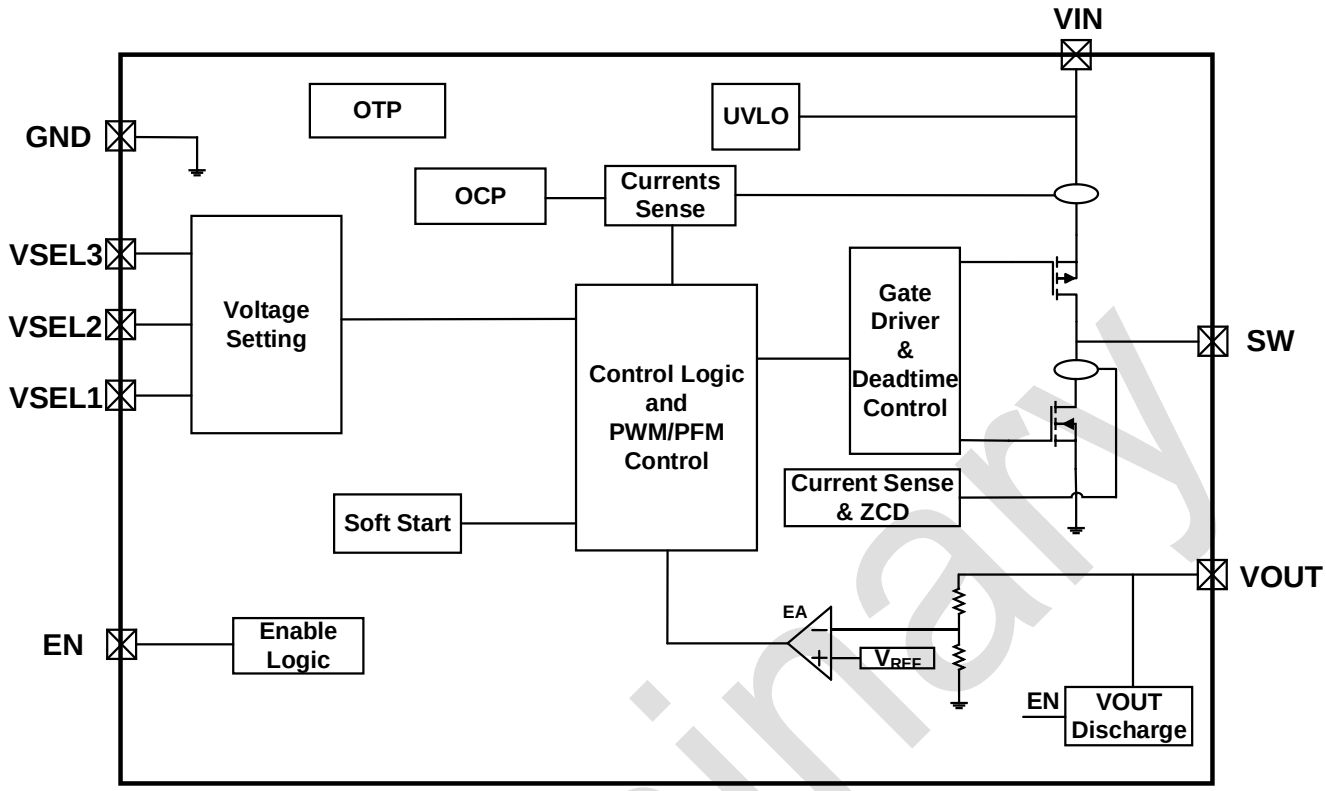

Figure 4 Block Diagram

Typical Applications

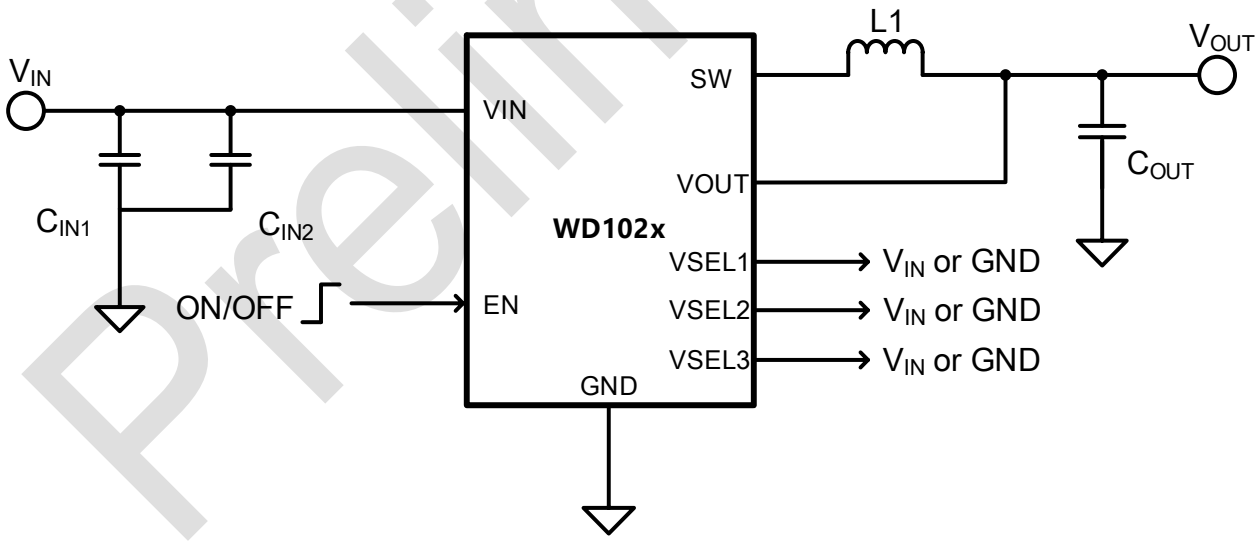

Figure 5 Typical Applications

Table 3 Component List for Typical Performance

Item	Value	Package	Part Number	Manufacturer
CIN1	47 µF	0805/X5R/10v	GRM21BR61A476ME15L	Murata
CIN2	4.7 µF	0402/X5R/10v	CL05A475KP5NRNC	SAMSUNG
COUT	10 µF	0402/X5R/10v	LDK105CBJ106MVLF	TAIYO
L1	2.2 µH	2520	1239AS-H-2R2M	Murata

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Table 4 VOUT Configuration

Pin			WD1020	WD1021
VSEL3	VSEL2	VSEL1	Vout (V)	Vout (V)
0	0	0	1.2	0.7
0	0	1	1.5	1
0	1	0	1.8	1.3
0	1	1	2.1	0.75
1	0	0	2.5	1.9
1	0	1	2.8	1.05
1	1	0	3	2.9
1	1	1	3.3	3.1

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses exceeding the range in Table 5 might cause substantial damage to the device. Functional operation of the device under other conditions is not implied. Prolonged exposure to extreme conditions might affect device reliability.

Table 5

Parameter	Symbol	Condition	Min.	Max.	Unit
VIN, SW, EN, VSEL1, VSEL2, VSEL3, VOUT	-	-	-0.3	6.0	V
Continuous Power Dissipation[1]	P_D	-	-	0.84	W
Maximum Junction Temperature	T_{J-MAX}	-	-	+150	°C
Junction-to-Ambient Thermal Resistance[2]	$R_{\theta JA}$	-	-	118.5	°C/W
Maximum Lead Temperature	T_L	Soldering, 10s	-	+260	°C
Operating Ambient Temperature	T_A	-	-40	85	°C
Storage Temperature	T_{stg}	-	-65	+150	°C
ESD Classification	HBM	-	-	±2000	V
	CDM	-	-	±2000	V

[1] Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages typically at T_J = 150°C and disengages typically at T_J = 125°C.

[2] Junction-to-ambient thermal resistance ($R_{\theta JA}$) is taken from a thermal modeling result and performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7.

Recommended Operation Conditions

Table 6

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Input Voltage	VIN	-	2.2	-	5.5	V
Junction Temperature Range	T_J	-	-40	-	125	°C
Operating ambient temperature	T_A	-	-40	-	85	°C

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Electrical Characteristics

V_{IN} = 3.6 V, C_{IN1}= 47 µF, C_{IN2}= 4.7 µF, C_{OUT} = 10 µF, L1 = 2.2 µH, T_A = 25°C, unless otherwise specified.

Table 7

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Buck Regulator						
Under-Voltage Lockout Rising Threshold	V_{UVLOR}			2	2.15	V
Under-Voltage Lockout Hysteresis	V_{UVLO_HYS}			0.1	0.4	V
V_{OUT} Voltage Accuracy	V_{OUT_ACC10}	V_{OUT} = 1.8 V, I_{OUT} = 10 mA	-2.5		2.5	%
	V_{OUT_ACC100}	V_{OUT} = 1.8 V, I_{OUT} = 100 mA	-2		2	
Input Quiescent Current	I_{QVIN}	V_{OUT} = 1.8 V, I_{OUT} = 0 A, EN = V_{IN}, non-switching		360	800	nA
	I_{QSW}	V_{OUT} = 1.8 V, I_{OUT} = 0 A, EN = V_{IN}, switching		630	1200	
Shutdown Current	I_{SHDN}	EN = GND		0.02	1	uA
Switching Frequency	f_{SW}	V_{OUT} = 1.8 V, CCM mode		0.9		MHz
HS Current Limit	I_{CLUG}	WD1020	1			A
		WD1021	0.64			
LS Current Limit	I_{CLLG}	WD1020	0.8	1	1.2	A
		WD1021	0.48	0.6	0.72	
HS R_{ON}	RON_UG	I_{OUT} = 50 mA		350		mΩ
LS R_{ON}	RON_LG	I_{OUT} = 50 mA		250		mΩ
Output Discharge RON	RON_DIS	EN = GND, I_{OUT} = −10 mA		10		Ω
VOUT Pin Input Leakage	I_{VOUT}	V_{OUT} = 2 V, EN = V_{IN}		95		nA
VOUT Minimum On Time	t_{ON_MIN}			100		ns
Line Regulation	$V_{OUT\_LineReg}$	V_{OUT} = 1.8 V, I_{OUT} = 100 mA, V_{IN} = 2.2 V to 5.5 V		0.23		%/V
Load Regulation	$V_{OUT\_LoadReg}$	V_{OUT} = 1.8 V, including PFM operation		0.003		%/mA
	$V_{OUT\_LoadReg}$	V_{OUT} = 1.8 V, only CCM operation		0.0003		
Over-Temperature Protection	T_{OTP}	I_{OUT} = 10 mA		140		°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}			25		°C
Timing						
Regulator Start Up Delay Time	t_{SS_EN}	I_{OUT} = 0 mA, EN = GND to V_{IN}, V_{OUT} starts rising		1		ms
Regulator Soft Start Time	t_{SS}	V_{OUT} = 1.8 V, I_{OUT} = 10 mA, EN = V_{IN}		1.4		ms
Logic Input (EN, VSEL1, VSEL2, and VSEL3)						
Input High Threshold	V_{IH}	V_{IN} = 2.2 V to 5.5 V	1.2			V
Input Low Threshold	V_{IL}	V_{IN} = 2.2 V to 5.5 V			0.4	V

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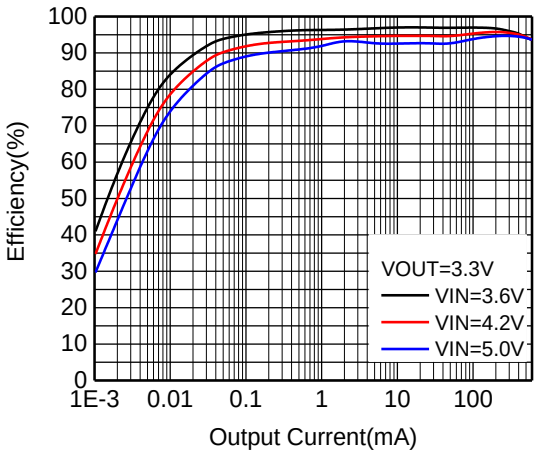
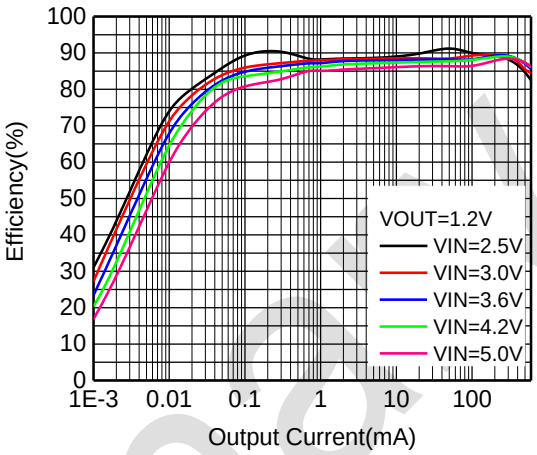
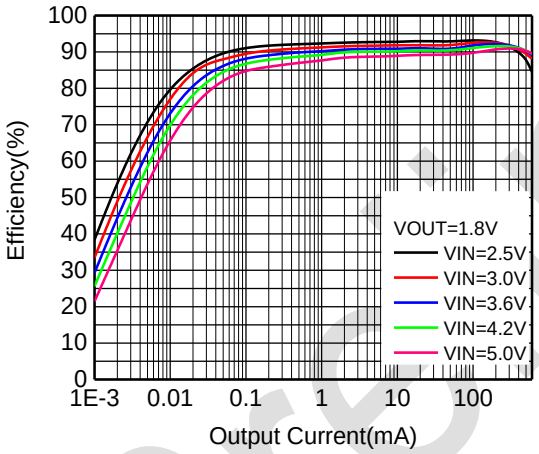
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Pin Bias Current	I_{IN}			10		nA

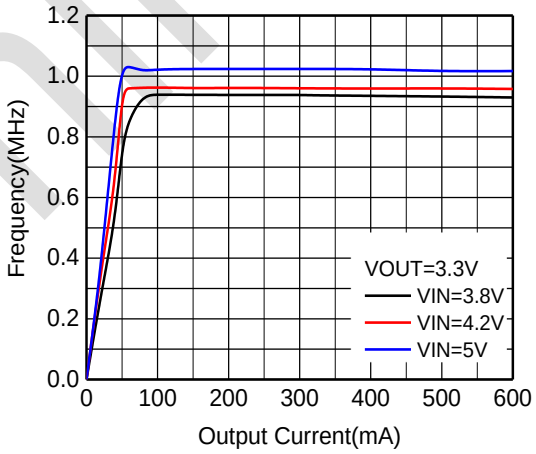
Typical Characteristics

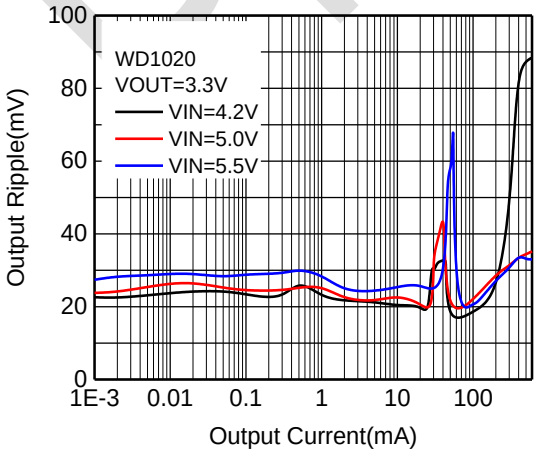
Ta=25°C, V_{IN}=V_{EN}=3.6 V, L1=2.2 µH, C_{IN1}=47 µF, C_{IN2} = 4.7 µF, C_{OUT}=10 µF, unless otherwise noted.

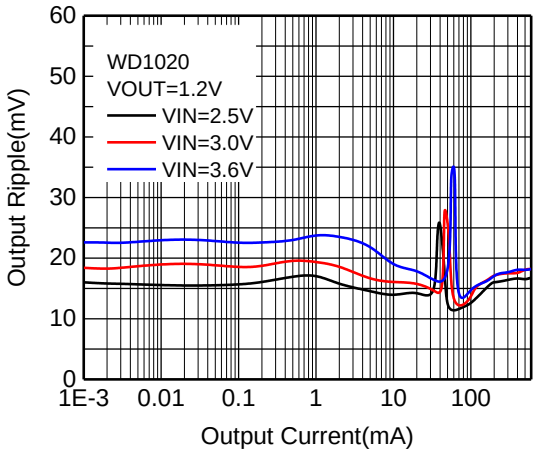












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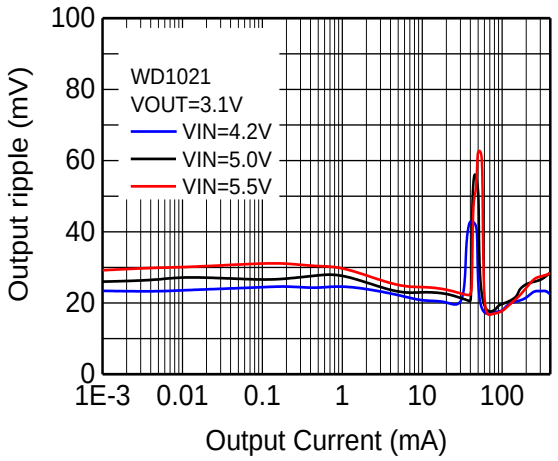
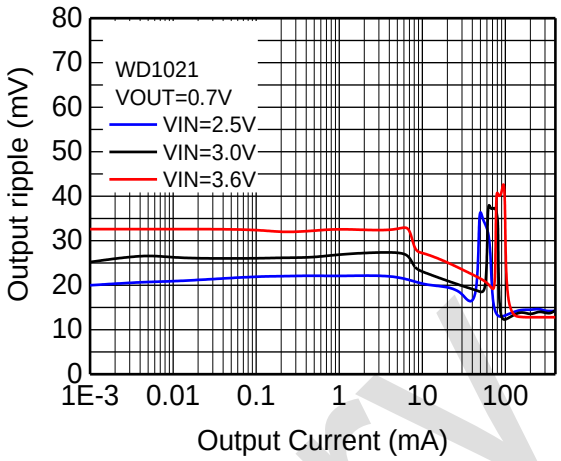
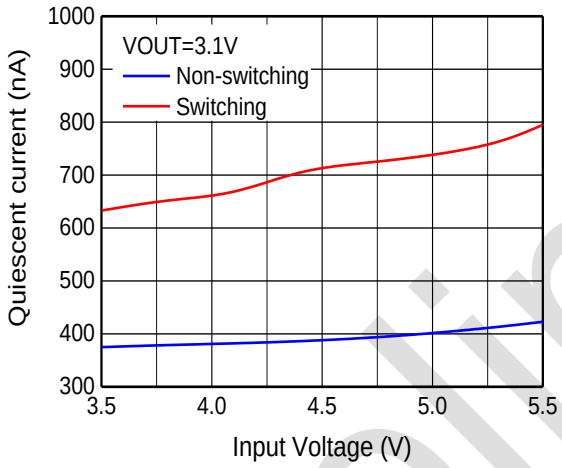
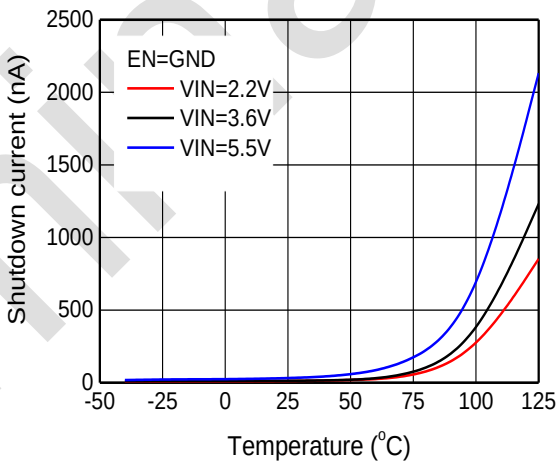
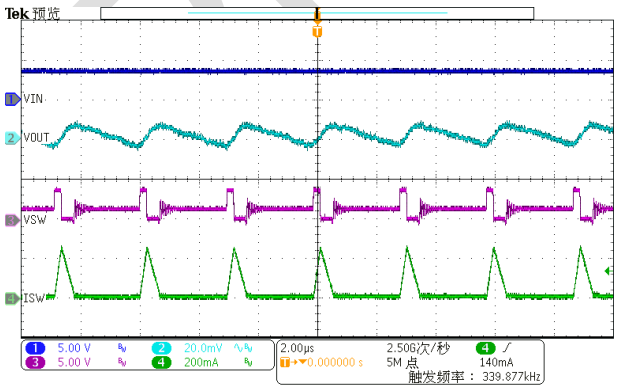


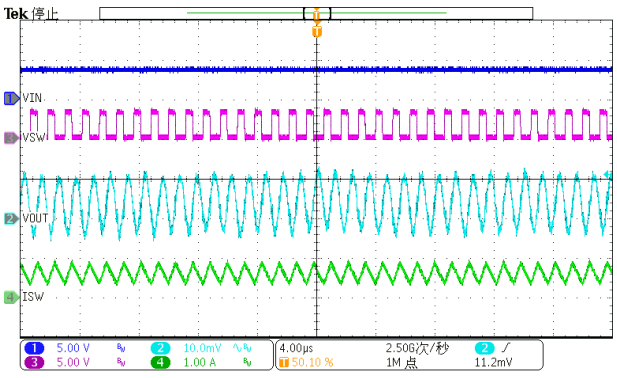








PFM, VIN=3.6 V, VOUT=1.2 V, IO=30 mA



PWM, VIN=3.6 V, VOUT=1.2V, IO=600 mA

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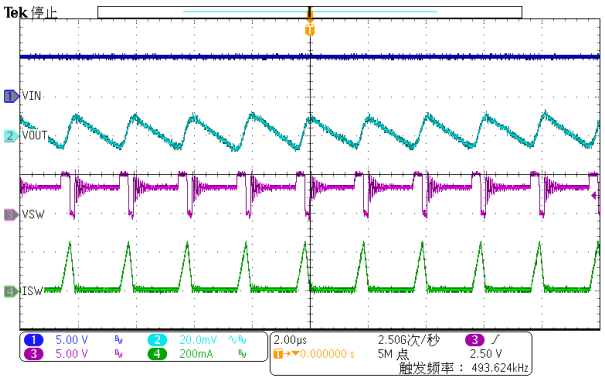
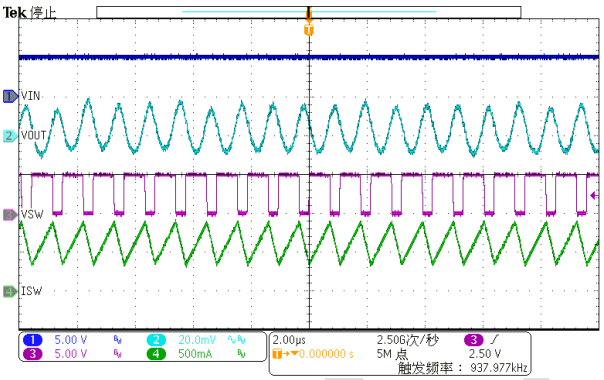
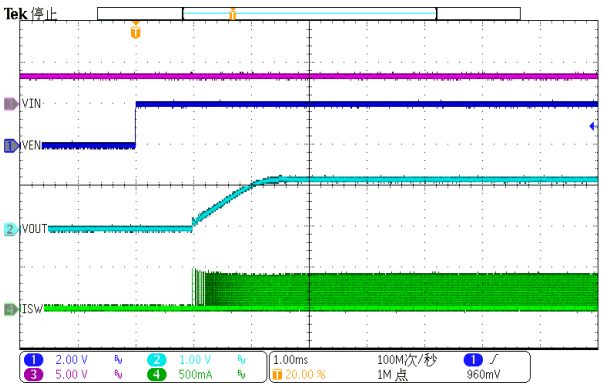


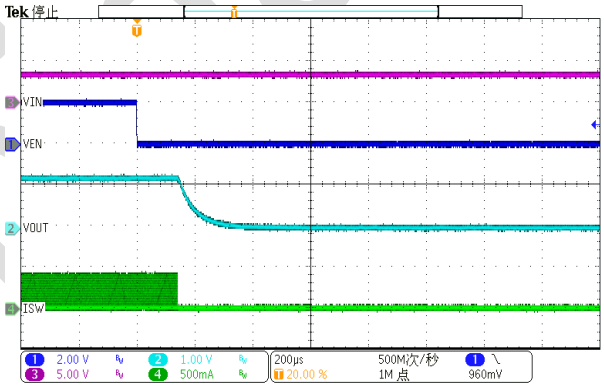
PFM, VIN=5 V, VOUT=3.3 V, IO=30 mA



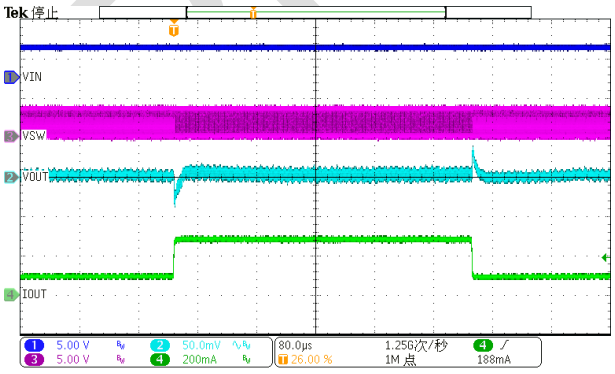
PWM, VIN=5 V, VOUT=3.3 V, IO=600 mA



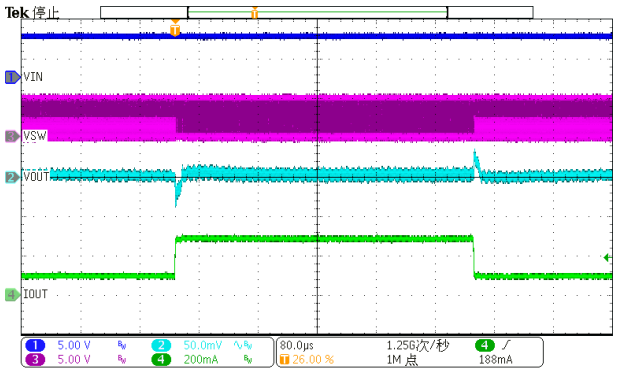
Startup, VIN=3.6 V, VOUT=1.2 V, IO=100 mA



Shut down, VIN=3.6 V, VOUT=1.2 V, IO=100 mA



Load Transient, VIN=3.6 V, VOUT=1.2 V, IO=0.1 A to 0.29 A



Load Transient, VIN=5 V, VOUT=1.2 V, IO=0.1 A to 0.29 A

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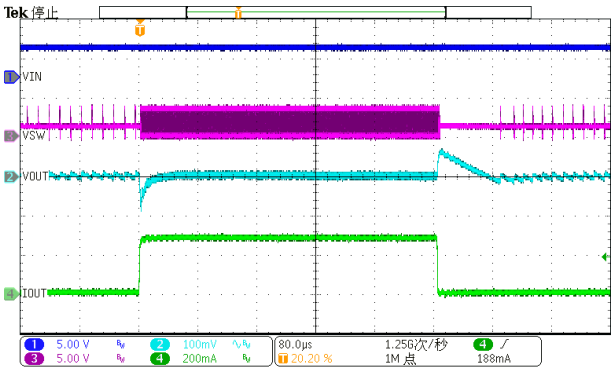

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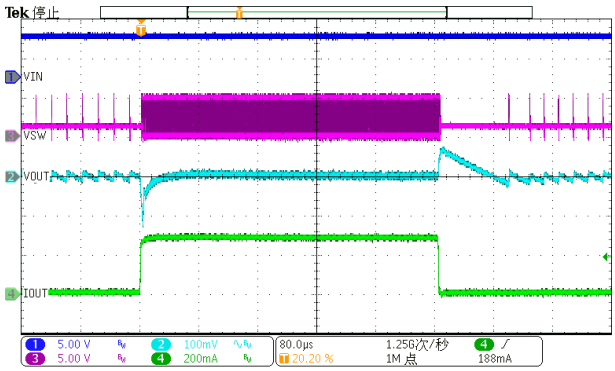
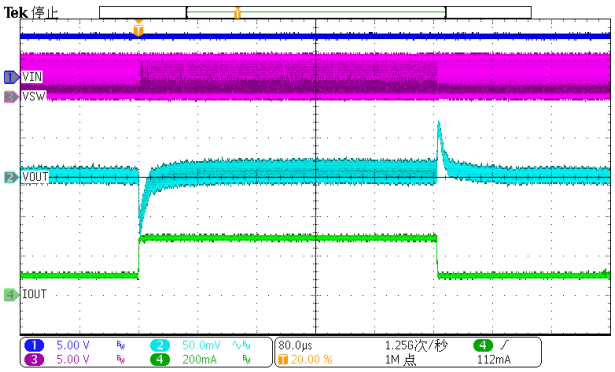
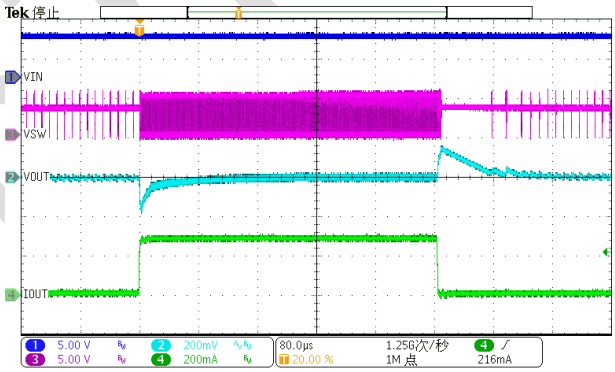


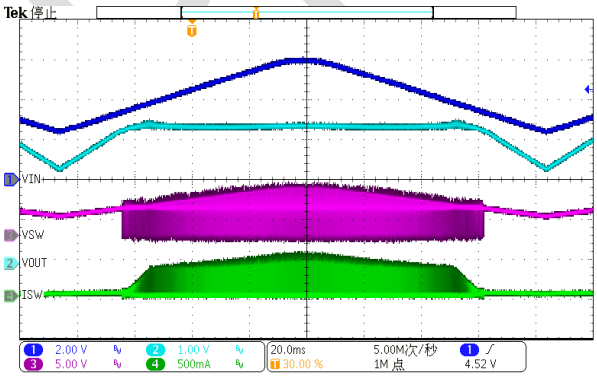
Load Transient, VIN=5 V, VOUT=1.2 V, IO=5 mA to 0.29 A



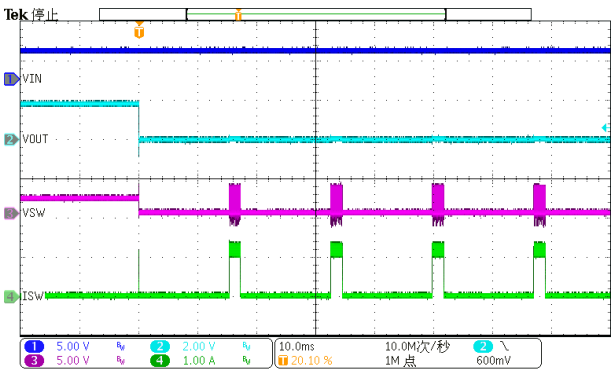
Load Transient, VIN=5 V, VOUT=3.3 V, IO=0.1 A to 0.29 A



Load Transient, VIN=5 V, VOUT=3.3 V, IO=5 mA to 0.29 A



100% Duty Cycle Entry and Leave Operation, IO=30 mA



VIN=3.6 V, VOUT=1.8 V, IO = 0 to short circuit.

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Operation Information

Device Information

The WD1020 and WD1021 are peak-current-mode switching buck converters with ultra-low quiescent current of typical 360 nA. The WD1020 and WD1021 support an input range from 2.2 V to 5.5 V. The devices support programmable output voltage defined by the VSELx pin with output current up to 600 mA, peak to 1.2A for the WD1020 and DC current up to 400 mA, peak to 0.8 A for the WD1021. The WD1020 and the WD1021 provide Over-Temperature Protection (OTP) and Over-Current Protection (OCP) mechanisms to prevent the device from damage in abnormal operations. The devices integrate internal compensation to minimize external component count. If the EN voltage is logic low, the IC is shut down with typically very low input supply current 0.02 µA.

Enable

The devices are enabled or disabled by the EN pin. When the EN pin is high, the IC goes to normal operation. When the EN pin is low, the IC goes to the shutdown mode and stops switching. Internal control circuitry is turned off and the discharge function is triggered. The discharge function closes typically after 10 ms. If systems need the EN toggle, then EN turn-off time must be longer than 200 µs for internal circuit reset.

UVLO Protection

To protect the chip from operating at insufficient supply voltage, the UVLO is needed. When the input voltage is lower than the UVLO falling threshold voltage, the device is lockout.

Output Voltage Selection

The WD1020 and the WD1021 provide up to eight-level output voltages which can be programmed through the voltage select pin from VSEL1 to VSEL3. Table 4 indicates the setting for individual output voltage.

100% Duty Cycle Operation

The converter enters 100% duty cycle operation automatically once the input voltage decreases close to V_{OUT}.

OCP

The OCP function is implemented by the HS and the LS. When the inductor current reaches the HS current limit threshold, the high-side MOSFET is turned off. The low-side MOSFET turns on to discharge the inductor current until the inductor current trips below the LS current limit threshold. After the HS current limit reaches, the maximum inductor current is decided by the current rising rate of the inductor and the response delay time of the internal network.

OTP

When the junction temperature exceeds typically the OTP threshold 140°C, the IC shuts down the switching. Once the junction temperature is typically lower than 115°C, the converter resumes switching.

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Application Information

Inductor Selection

The power inductor is recommended to be 2.2 µH. Inductor saturation current rating needs to match the OCP design. In applications, an inductor with low DCR is recommended for good performance and efficiency.

CIN and COUT Selection

The input capacitance, C_{IN}, is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low Effective Series Resistance (ESR) input capacitor matching the maximum RMS current needs to be used. The RMS current is given by:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

The formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT} / 2$. The worst case is commonly used for design because even significant deviations do not offer much relief. Choose a capacitor rated at a higher temperature than required.

Paralleled capacitors might be used to meet size or height requirements in the design.

The selection of C_{OUT} is determined by the ESR that is required to minimize voltage ripple and load step transients, as well as the amount of ceramic capacitance that is necessary to ensure that the control loop is stable. Loop stability is checked by viewing the load transient response.

The output ripple, ΔV_{OUT}, is determined by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right)$$

For the best performance, use ceramic capacitors for both input and output. Capacitors with X5R or even X7R ceramic dielectrics are recommended because they are stable with temperature fluctuations. The DC bias of ceramic capacitors also needs to be considered when evaluating the effective capacitance.

Thermal Considerations

In case of permanent damage to the device, the junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$ listed in Table 5 . The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation is calculated using the following formula:

$$P_{D\,(MAX)} = (T_{J\,(MAX)} - T_A) / \theta_{JA}$$

Where $T_{J\,(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

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PC Board Layout Considerations

Good circuit board layout aids in extracting the most performance from the WD1020 and the WD1021. Poor circuit layout degrades the output current capability, output ripple, and EMI or EMC performance. Good layouts for the WD1020 and the WD1021 are implemented by following design rules below:

1. Place the WD1020 or the WD1021, inductor, and filter capacitors close to each other and make the traces short. The traces between these components carry high switching current and act as antennae. Place the input filter capacitor close to the VIN and the GND pad.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the WD1020 or WD1021 and inductor, to the output filter capacitor. Current flows back through the ground, forming a current loop. In the second half of each cycle, current is pulled up from the ground, through the WD1020 or the WD1021 by the inductor, to the output filter capacitor. Current flows back through the ground, forming a second current loop. Rout current loops so the current curls in the same direction, preventing magnetic field reversal between the two half-cycles and reducing radiated noise.
3. Connect the ground pad of the WD1020 or the WD1021 to filter capacitors using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground plane (if one is used) with several vias to reduce ground plane noise by preventing the switching current from circulating through the ground plane. It also reduces ground bounce at the WD1020 or the WD1021 by giving the device a low-impedance ground connection.
4. The VOUT sense trace is a sensitive high-impedance line. Route the trace away from noisy traces and components such as SW net and external noise sources. The VOUT sense trace also needs to be connected to the output capacitor.

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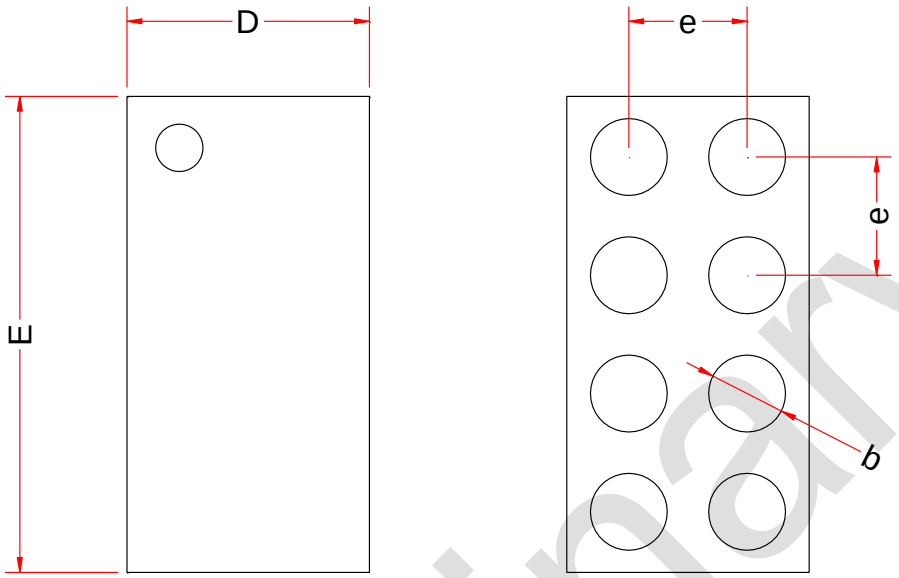
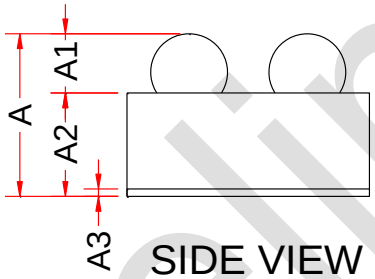
Package Outline Dimensions

CSP-8L





Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.505	0.550	0.595
A1	0.180	0.200	0.220
A2	0.325	0.350	0.375
A3		0.025	
E	1.580	1.610	1.640
D	0.790	0.820	0.850
b	0.240	0.260	0.280
e		0.400 BSC	

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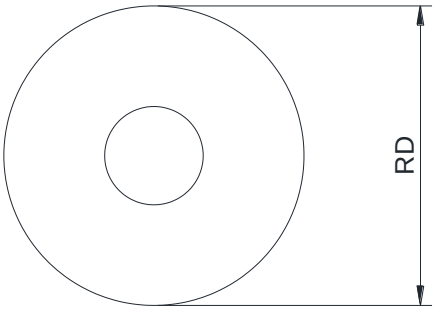
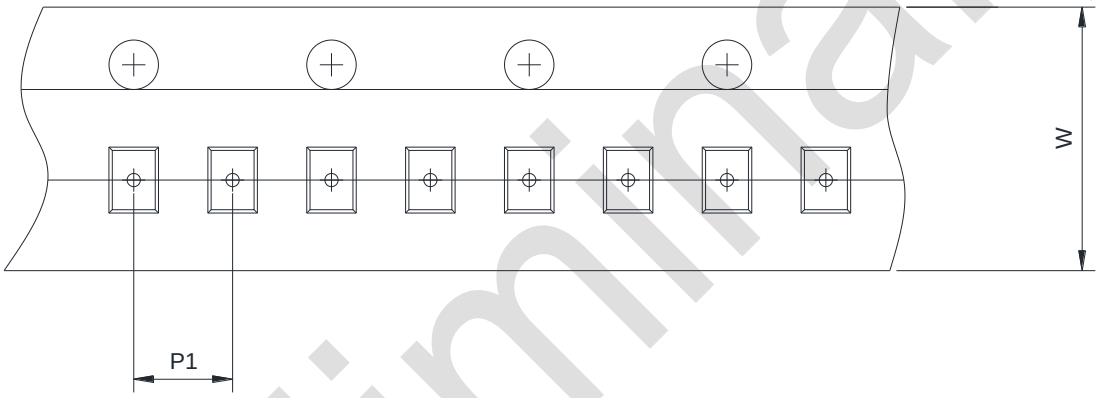
Tape and Reel Information

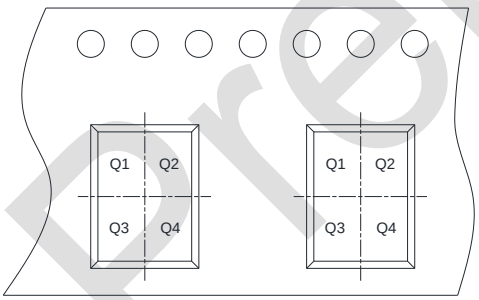
Reel Dimensions



Tape Dimensions



Quadrant Assignments for PIN1 Orientation in Tape



User Direction of Feed

RD	Reel dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4

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