

## WD1072VA, WD1072D

### 2-A Step-Down Converter with Forced PWM Feature

#### Descriptions

The WD1072 is a synchronous step-down DC-DC converter optimized for high efficiency and compact solution size. The device integrates switches capable of delivering an output current up to 2 A. At the whole load range, the device operates in the quasi-fixed frequency constant on time mode with 1.5 MHz switching frequency. In shutdown, the current consumption is less than 2  $\mu$ A.

An internal soft start circuit limits the inrush current during startup. The WD1071 also has built-in features including over current protection and thermal shutdown protection.

The WD1072 is available in an SOT-563 and a DFN1616 package. Standard products are Pb-free and Halogen-free.

#### Features

- Input voltage range from 2.5 V to 5.5 V
- Forced PWM to reduce output voltage ripple
- Up to 95% efficiency
- Integrate 125 m $\Omega$  (high side) and 65 m $\Omega$  (low side) low R<sub>DS(ON)</sub> power MOSFETs
- Adjustable output voltage from 0.6 V to VIN
- 100% duty cycle for the lowest dropout
- 1.5MHz typical switching frequency
- Over-current protection and hiccup
- Thermal shutdown protection

#### Applications

- General purpose POL supplies
- Set top boxes
- Network video cameras
- Wireless routers
- Solid state drivers and hard disk drivers

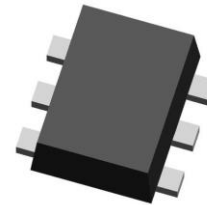


Figure 1 SOT-563

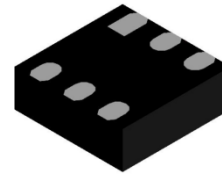
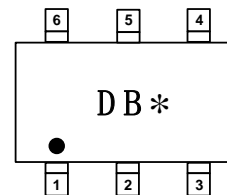
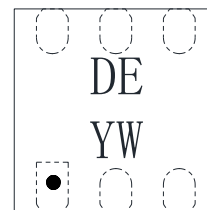


Figure 2 DFN1616



DB = Device name  
\* = Month code

Figure 3 Marking of the SOT-563



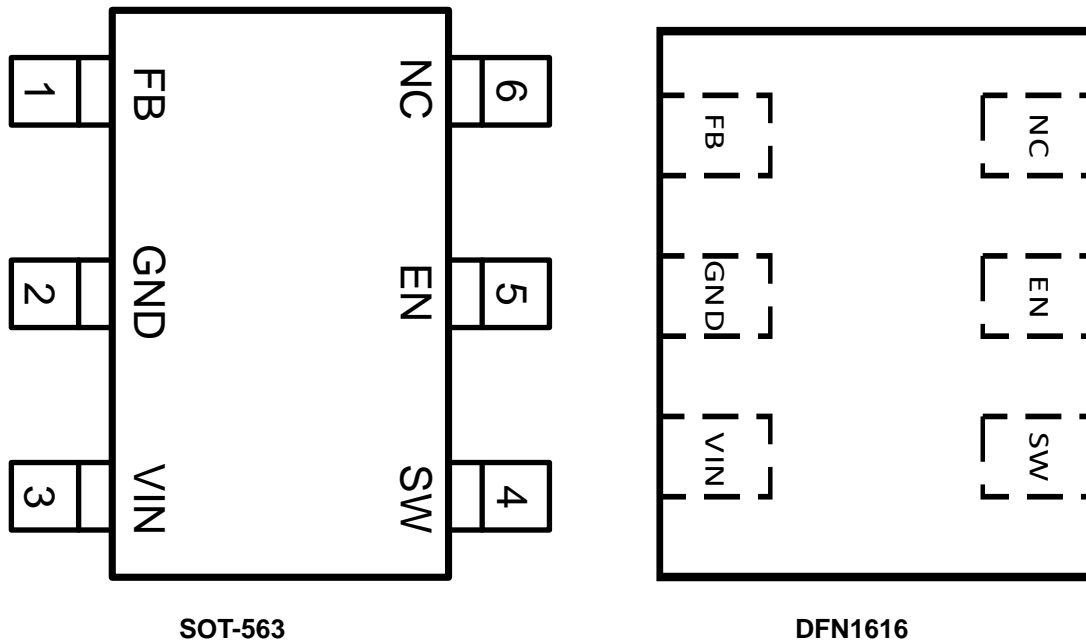
DE = Device name  
\* = Month code

Figure 4 Marking of the DFN1616

#### Order Information

Table 1

Device	Package	Shipping
WD1072VA-6/TR	SOT-563	3000/Reel&Tape
WD1072D-6/TR	DFN1616	3000/Reel&Tape

**Pin Information**

**Figure 5 Pin Configuration (Top View)**
**Table 2**

Pin	Symbol	Description
1	FB	Converter feedback input. Connect to output voltage with feedback resistor divider.
2	GND	System ground pin. Reference ground of the regulated output voltage: requires extra care during PCB layout. Connect to the GND with copper traces and vias.
3	VIN	Supply voltage pin. Requires a cap to decouple the input rail. Connect using a wide PCB trace.
4	SW	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter using a wide PCB trace to the pin.
5	EN	Device enable logic input. Logic high enables the device; logic low disables the device and turns it into shutdown. Do not leave floating. To activate high for automatic start-up, the EN can be connected to the VIN directly or through a resistor.
6	NC	No connection. Recommend connecting the pin to the ground net for better thermal performance.

Block Diagram

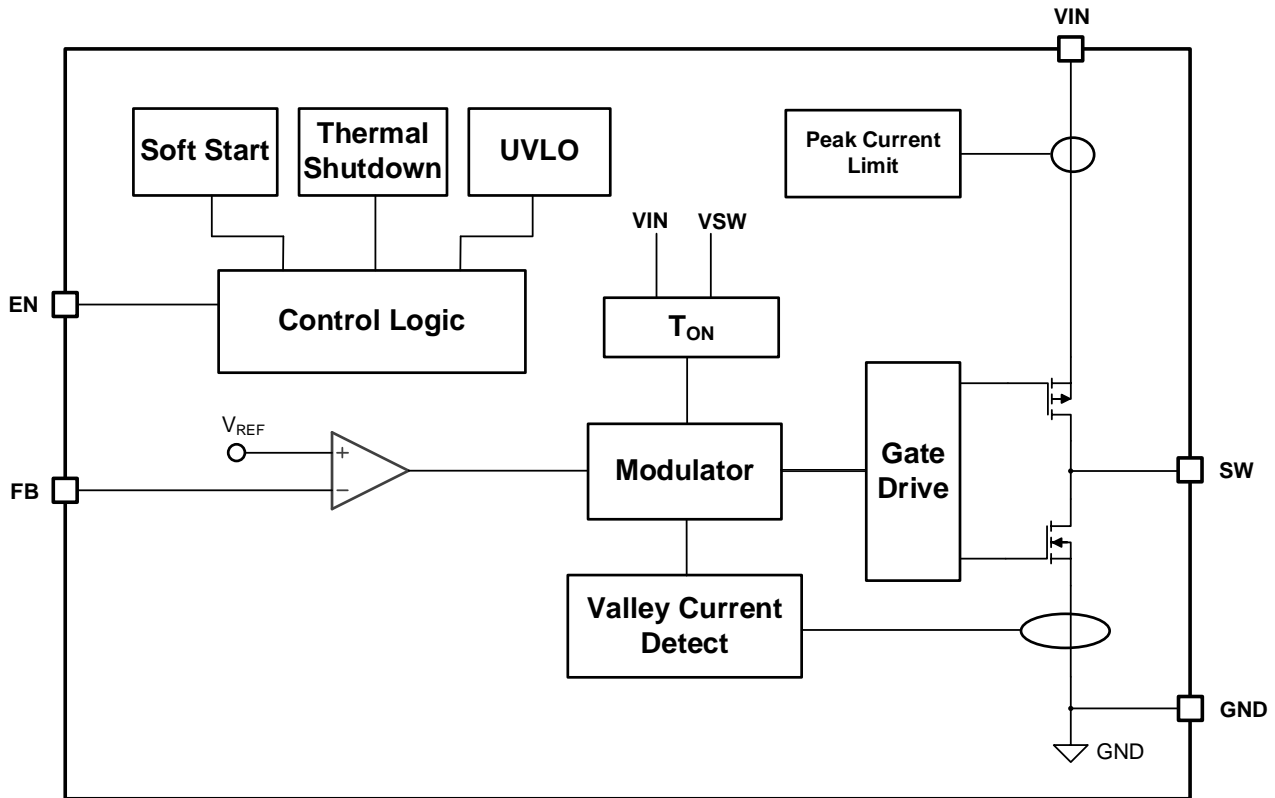


Figure 6 Block Diagram

Typical Applications

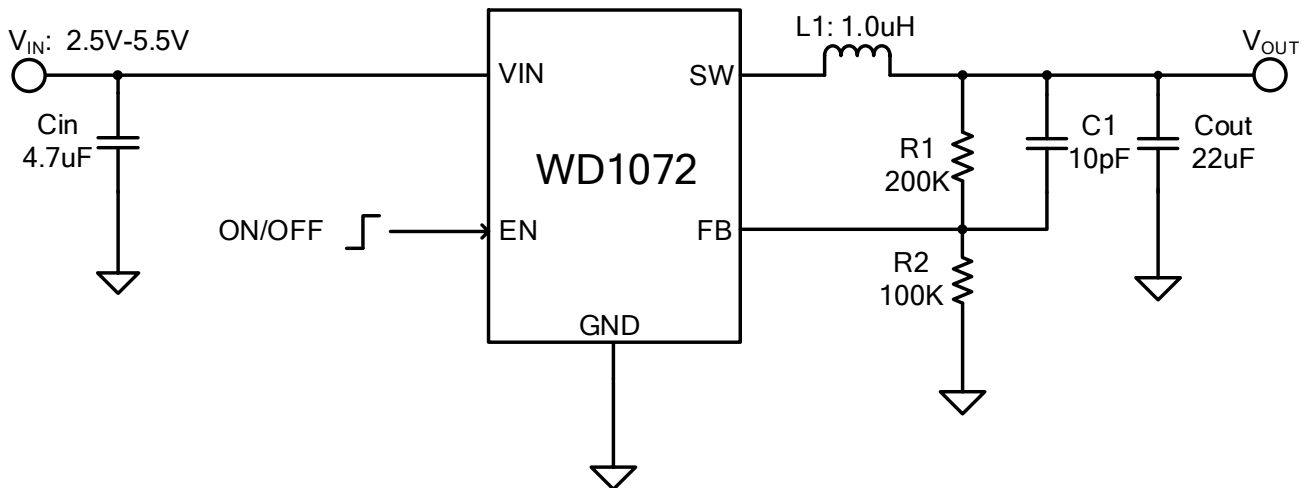


Figure 7 Typical Applications

## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses beyond the range in [table 3](#) might cause substantial damage to the device. Functional operation of the device under other conditions is not implied. Prolonged exposure to extreme conditions might affect device reliability.

**Table 3**

Parameter	Symbol	Condition	Min.	Max.	Unit
-	$V_{IN}, V_{EN}$		-0.3	6	V
Switch output	$V_{SW}$	DC	-0.3	$V_{IN}+0.3$	V
Switch output	$V_{SW}$	AC, less than 10ns	-3.0	9	V
Output voltage feedback	$V_{FB}$		-0.3	3	V
Operation junction temperature	$T_J$		-40	150	°C
-	$\theta_{JA}$			142	°C/W
	$\theta_{JC}$			51	
Storage Temperature	$T_{stg}$		-65	150	°C
Human Body Model (HBM)	HBM	Per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>		2000	V
Charged Device Model (CDM)	CDM	Per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>		500	V

## Recommended Operation Conditions

**Table 4**

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	$V_{IN}$		2.5		5.5	V
Output voltage	$V_{OUT}$		$V_{FB}$		$V_{IN}$	V
Output current	$I_{OUT}$		0		2	A
Operating junction temperature	$T_J$		-40	-	125	°C

## Electrical Characteristics

Ta=25°C, V<sub>IN</sub>=5 V, unless otherwise noted.<sup>(2)</sup>

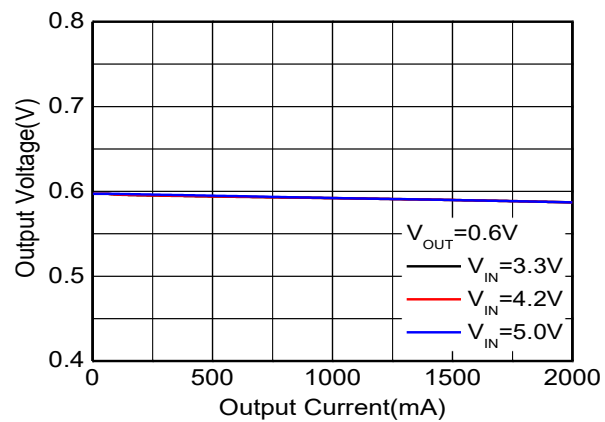
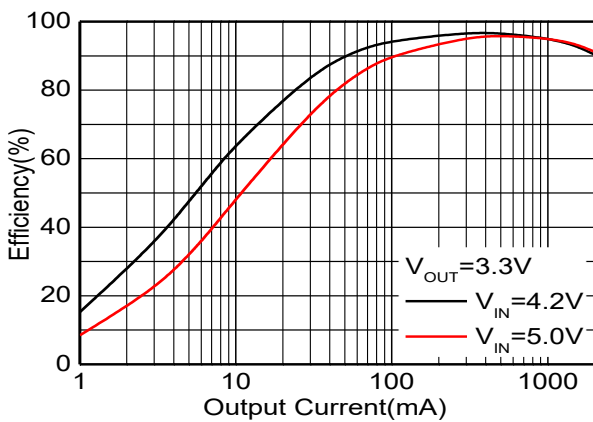
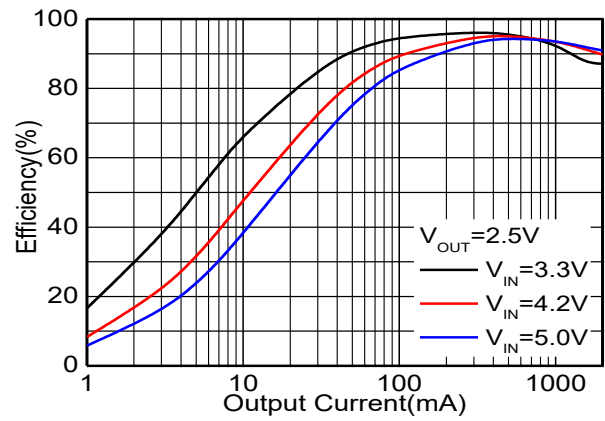
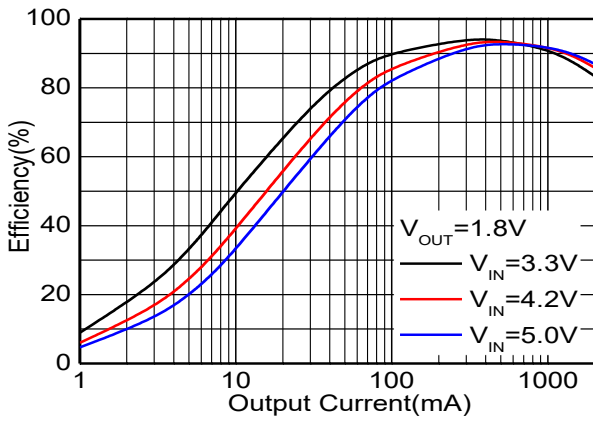
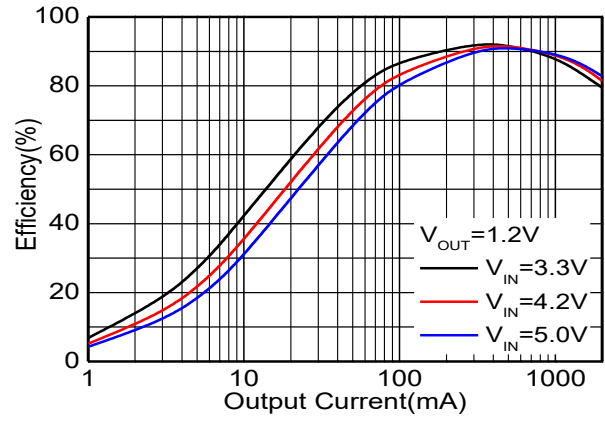
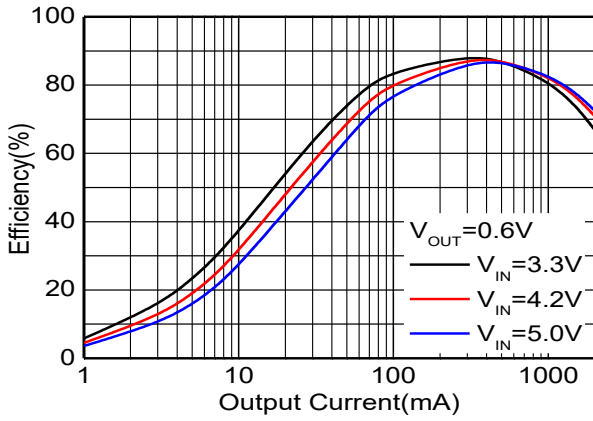
**Table 5**

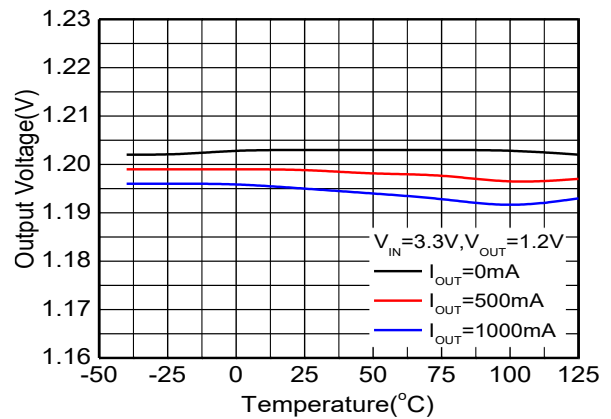
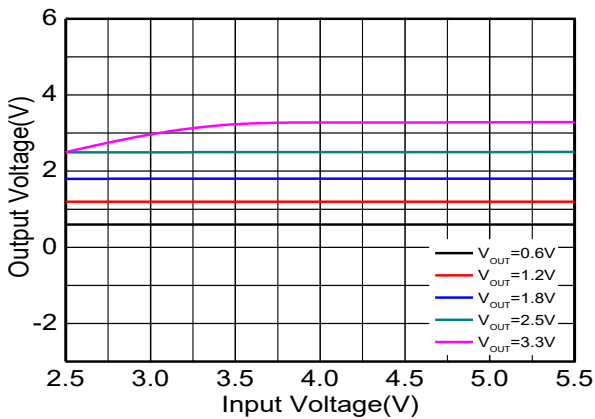
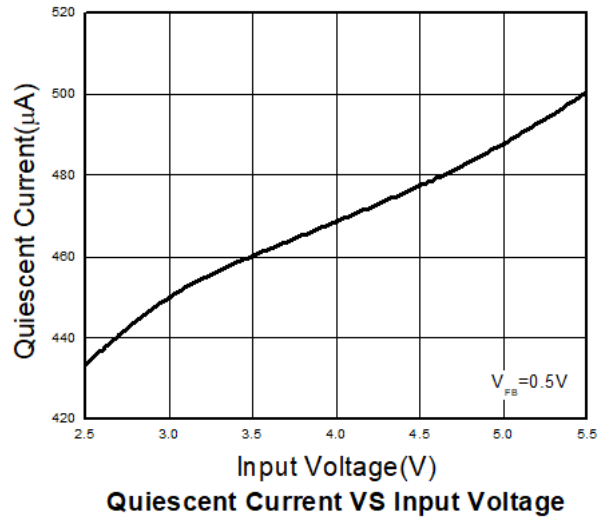
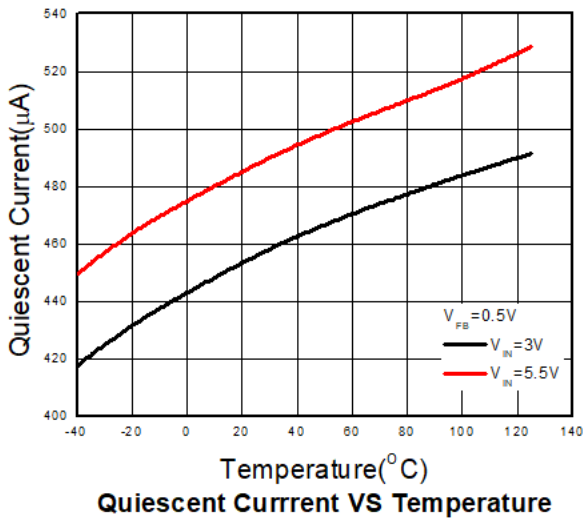
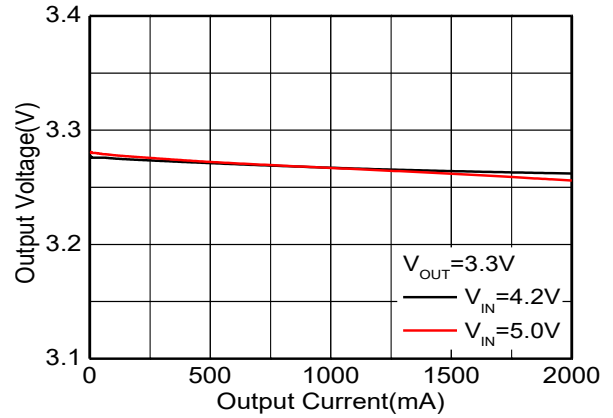
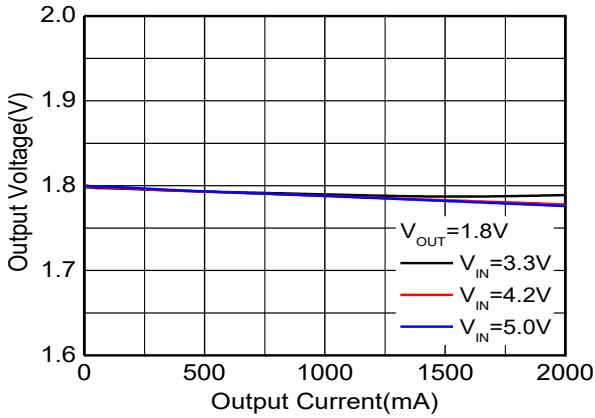
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current (shutdown)	I <sub>SD</sub>	V <sub>EN</sub> = 0 V		0.01	2	μA
Supply current (quiescent)	I <sub>Q</sub>	V <sub>EN</sub> = 2 V, V <sub>FB</sub> = 0.5 V		500		uA
HS switch-on resistance	R <sub>on_HS</sub>	I <sub>SW</sub> =100 mA, V <sub>IN</sub> =3.6 V		125		mΩ
LS switch-on resistance	R <sub>on_LS</sub>	I <sub>SW</sub> = -100 mA, V <sub>IN</sub> =3.6 V		65		mΩ
Current limit	I <sub>LIM</sub>	High-side FET current limit	3			A
Switching frequency	F <sub>SW</sub>			1500		kHz
Max duty cycle	D <sub>MAX</sub>		100			%
Feedback voltage	V <sub>REF</sub>	T <sub>J</sub> = 25°C	594	600	606	mV
		T <sub>J</sub> = -40°C to 125°C	588		612	
Feedback current	I <sub>FB</sub>	V <sub>FB</sub> =0.63 V		50	100	nA
EN rising threshold	V <sub>EN_RISING</sub>		1.2			V
EN falling threshold	V <sub>EN_FALLING</sub>				0.4	V
EN input current	I <sub>EN</sub>	V <sub>EN</sub> =2 V		0.4		μA
		V <sub>EN</sub> =0 V		0		
VIN under voltage lockout threshold	INUV <sub>TH</sub>	Rising		2.3	2.45	V
VIN under voltage lockout threshold hysteresis	INUV <sub>HYS</sub>			100		mV
Soft-Start period	T <sub>SS</sub>			1.2		ms
Thermal shutdown	T <sub>SD</sub>			160		°C
Thermal hysteresis	TSD <sub>HYS</sub>			25		°C

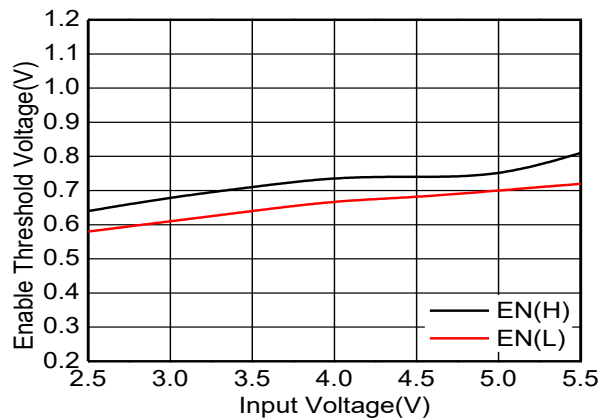
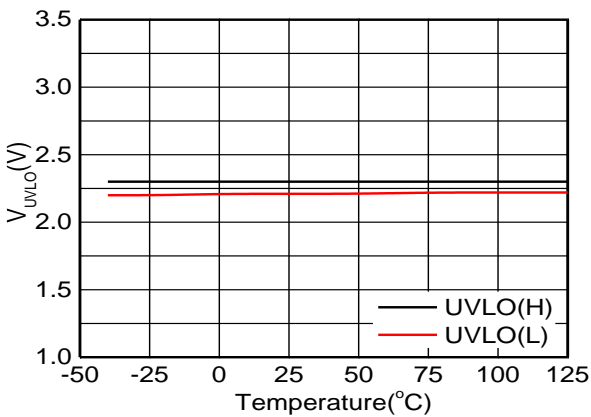
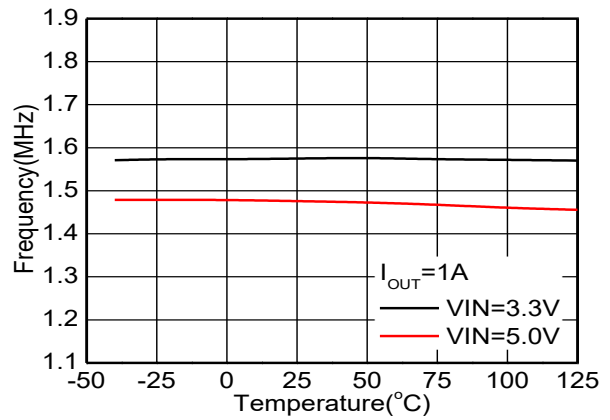
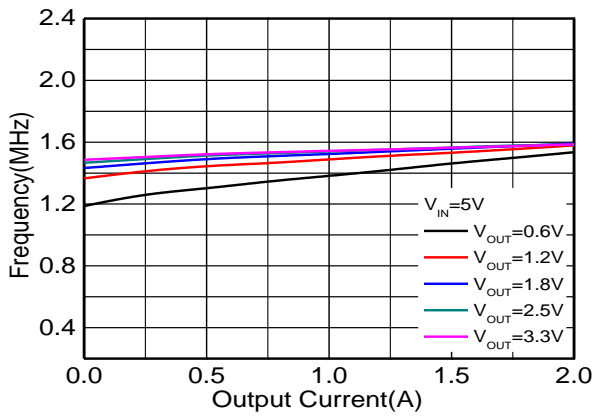
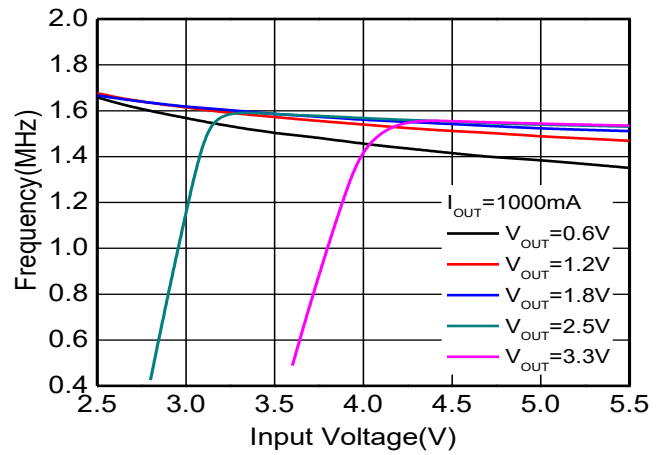
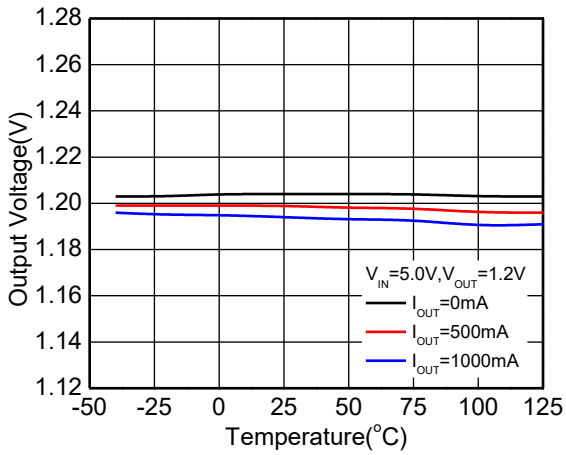
**Note (2):** Guaranteed by design and engineering sample characterization.

Typical Characteristics

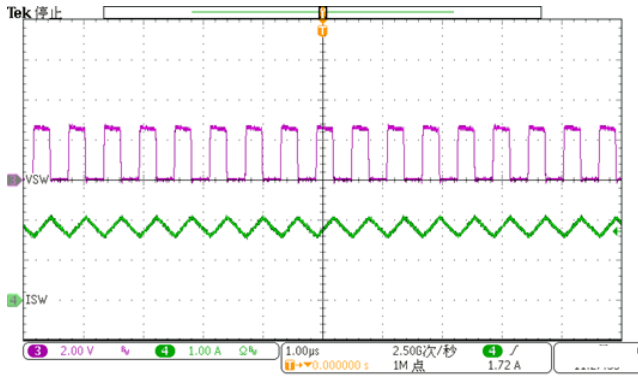
$V_{IN}=5\text{ V}$ ,  $V_{OUT}=1.8\text{ V}$ ,  $L=1.0\ \mu\text{H}$ ,  $C_{IN}=4.7\ \mu\text{F}$ ,  $C_{OUT}=22\ \mu\text{F}$ ,  $T_A=+25^\circ\text{C}$ , unless otherwise noted.



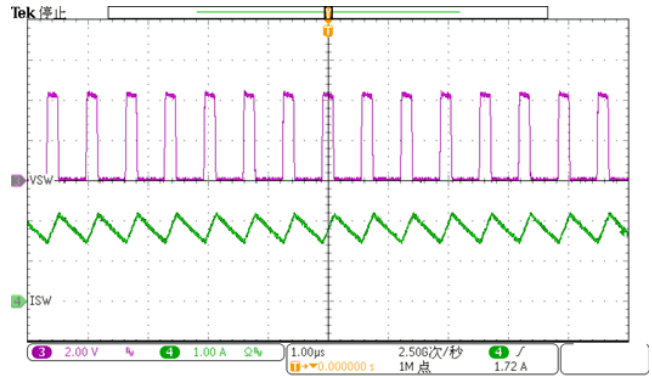




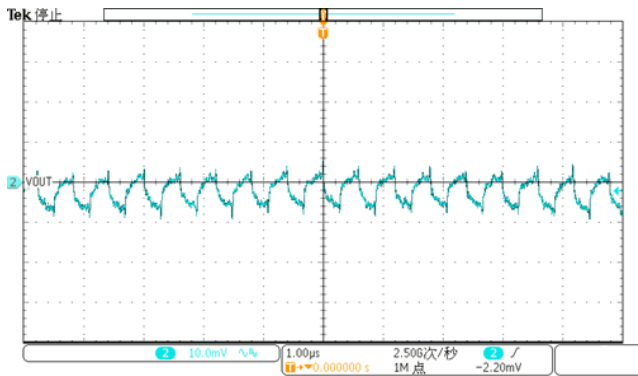




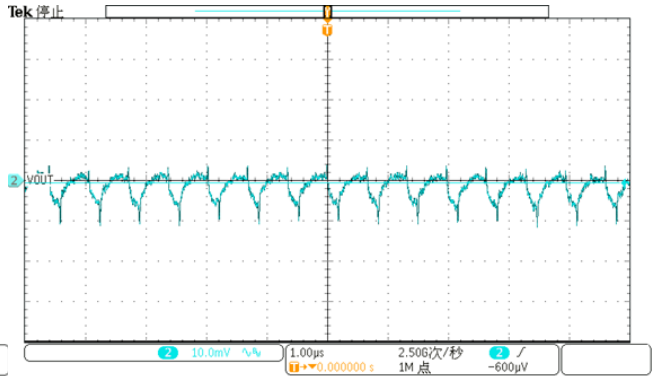
Switching waveform,  $V_{IN}=3.3\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=2\text{ A}$



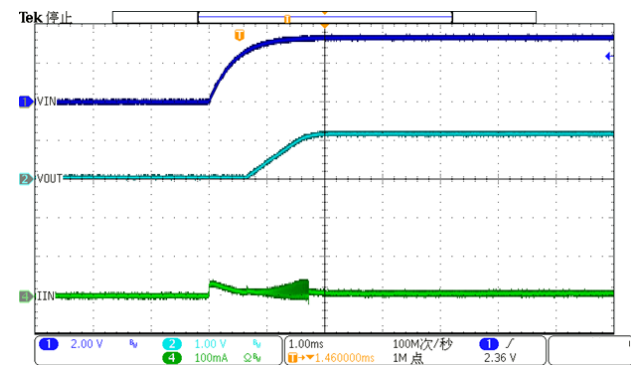
Switching waveform,  $V_{IN}=5.0\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=2\text{ A}$



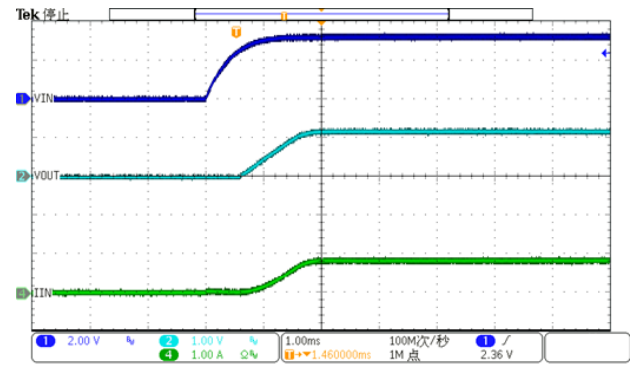
Ripple,  $V_{IN}=3.3\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=2\text{ A}$



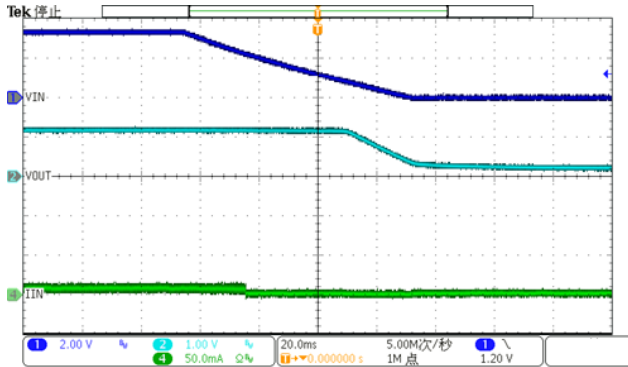
Ripple,  $V_{IN}=5.0\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=2\text{ A}$



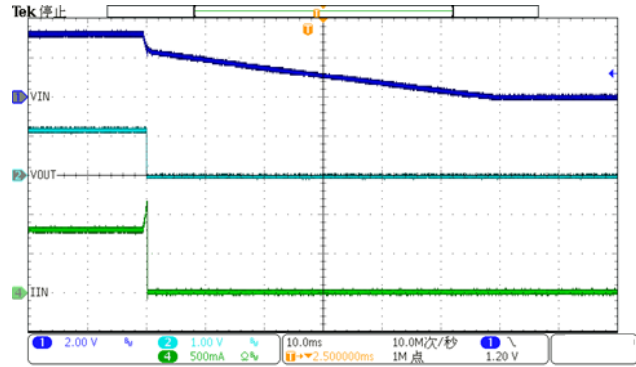
Start up from  $V_{IN}$ ,  $V_{IN}=3.3\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=0\text{ A}$



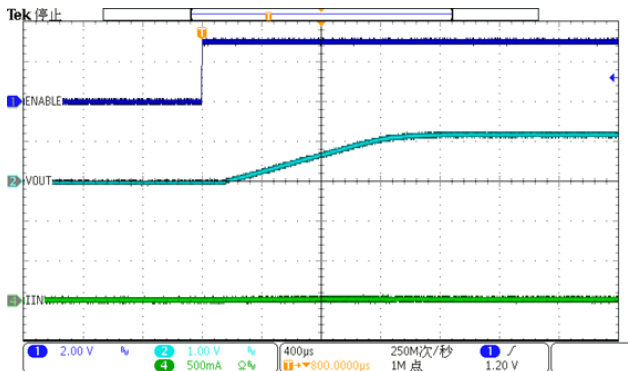
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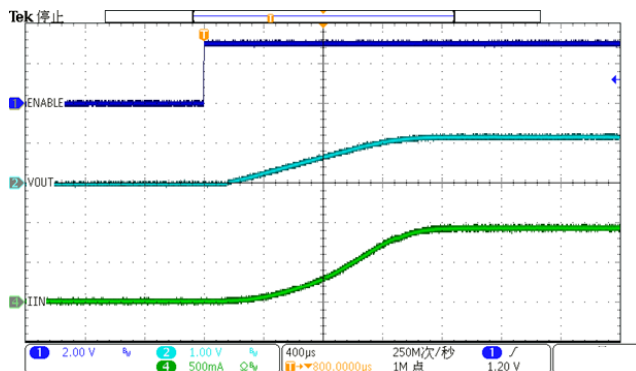
Shut down from  $V_{IN}$ ,  $V_{IN}=3.3\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=0\text{ A}$



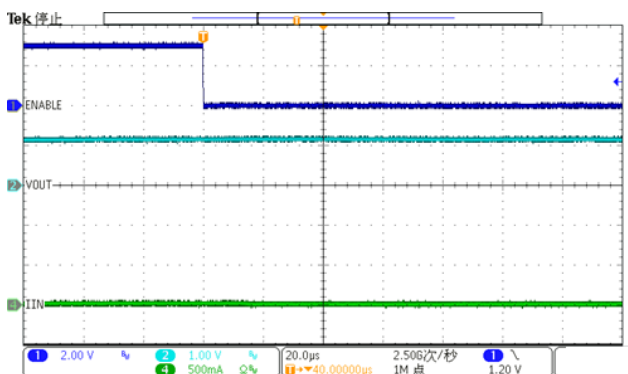
Shut down from  $V_{IN}$ ,  $V_{IN}=3.3\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=2\text{ A}$



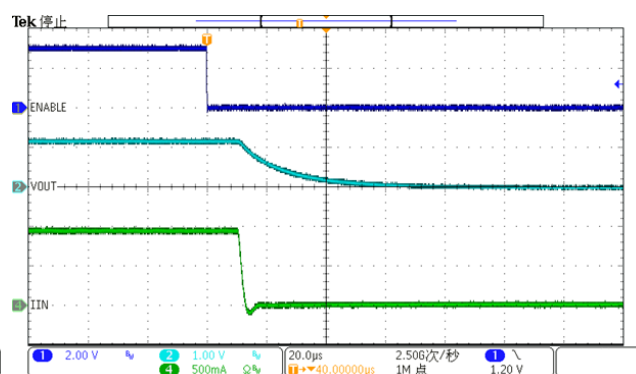
Start up from EN,  $V_{IN}=3.3\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=0\text{ A}$



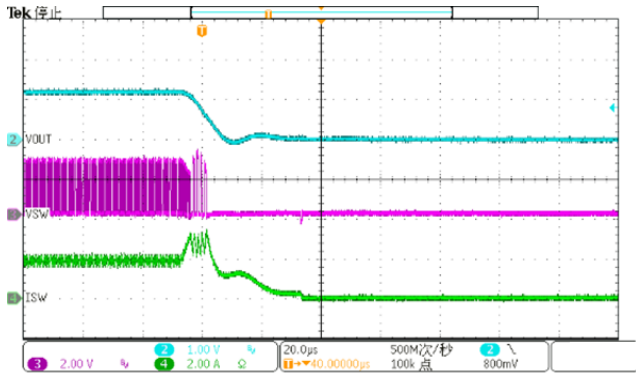
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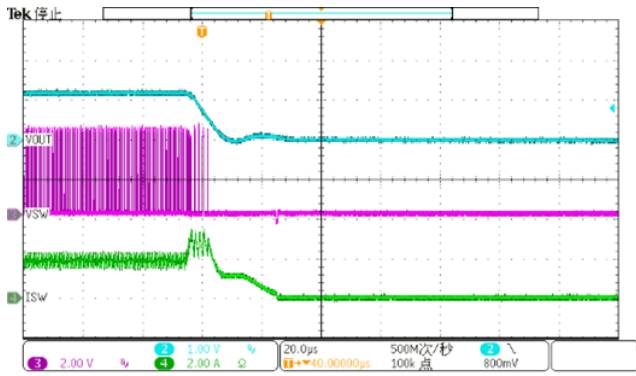
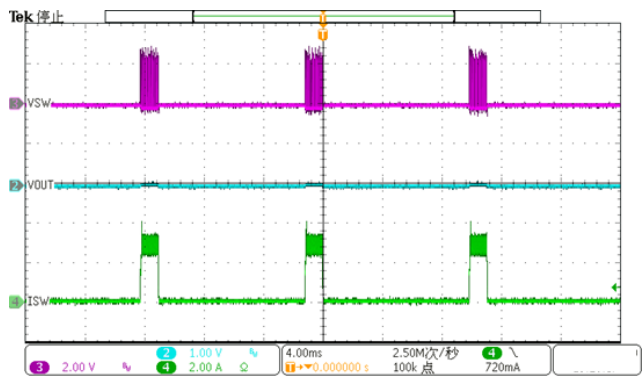
Shut down from EN,  $V_{IN}=3.3\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=0\text{ A}$



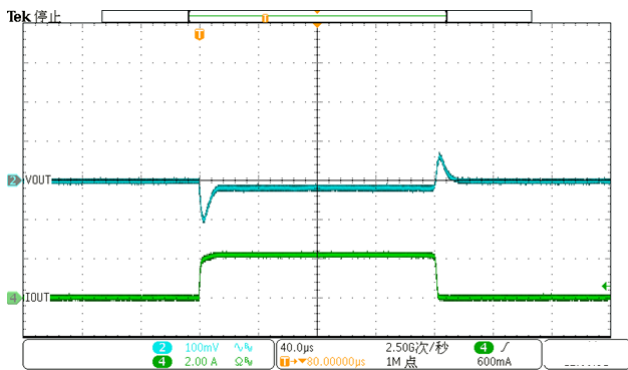
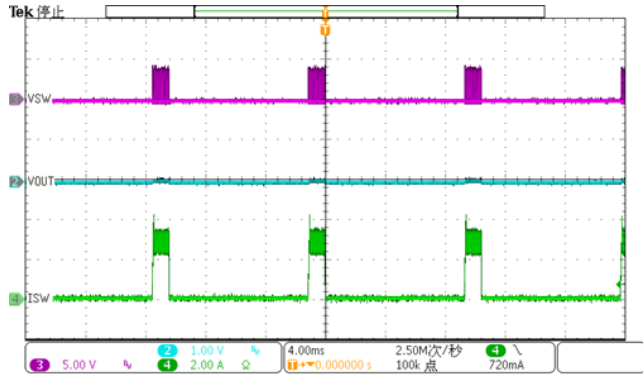
Shut down from EN,  $V_{IN}=3.3\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=2\text{ A}$



$V_{IN}=3.3\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=2\text{ A}$ ~Short to GND



$V_{IN}=5.0\text{ V}$ ,  $V_{OUT}=1.2\text{ V}$ ,  $I_{OUT}=2\text{ A}$ ~Short to GND



Load Transient,  $V_{IN}=3.3\text{ V}$ ,  $V_{OUT}=1.5\text{ V}$ ,  $I_{OUT}$  1 mA to 2000 mA

## Operation Information

The WD1072 is a high-efficiency FPWM synchronous step-down converter. The device operates with an adaptive on time with valley current control scheme. The device operates at typically 1.5 MHz frequency in a constant on time mode. Based on the  $V_{IN}/V_{OUT}$  ratio, the internal circuit sets required on time for high side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current.

### Enabling and Disabling the Device

The WD1072 is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

### 100% Duty Cycle Low Dropout Operation

The WD1072 offers 100% duty cycle operation mode. In the mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. Depending on the load current and output voltage, the minimum input voltage to maintain output regulation is calculated as below:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L)$$

where

- $R_{DS(ON)}$  = High side FET on-resistance
- $R_L$  = Inductor ohmic resistance (DCR)

### Soft Startup

After enabling the WD1072, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage in 1.2 ms typically. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device can start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

### Switch Current Limit

The switch current limit prevents the WD1072 from high inductor current. The limit also prevents the WD1072 from drawing excessive current from a battery or an input voltage rail. Excessive current might occur under a heavy load or shorted output circuit condition. The device adopts the peak current limit control by sensing the current of the high-side switch. Once the high-side switch current limit reaches, the high-side switch is turned off and the low-side switch is turned on to ramp down the inductor current with an adaptive off-time.

### Under Voltage Lockout

To avoid mis-operation of the WD1072 at low input voltages, the Under Voltage Lockout (UVLO) is implemented to shut down the device at voltages lower than the  $V_{UVLO}$  with  $V_{HYS\_UVLO}$  hysteresis.

### Thermal Shutdown

The WD1072 enters thermal shutdown if the junction temperature exceeds the thermal shutdown rising threshold,  $T_{JSD}$ . If the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

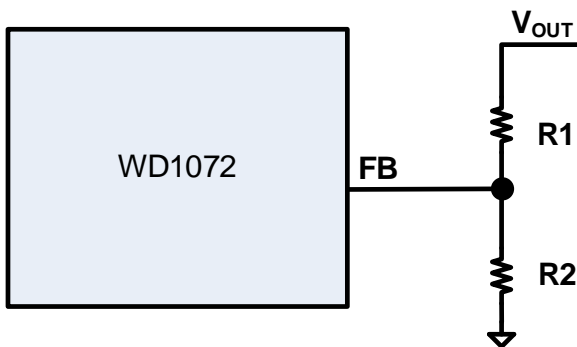
## Application Information

### Setting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation (1) to calculate the  $V_{OUT}$ . To improve efficiency at light loads, consider using larger value resistors. High resistance is more susceptible to noise and voltage errors from the FB input current are more noticeable.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

The feedback circuit is shown below:



### Setting the Inductor

An inductor is necessary to supply a constant current to the output load while being driven by the switched input voltage. A larger inductor results in less ripple current and a lower output ripple voltage. A larger inductor also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be between 30% and 40% of the maximum output current, and ensure that the peak inductor current is below the maximum switch current limit. The inductance value is calculated with Equation (2):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Where  $\Delta I_L$  is the peak-to-peak inductor ripple current. The inductor should not saturate under the

maximum inductor peak current. The peak inductor current is calculated with equation (3):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

### Selecting the Input Capacitor

The device requires an input decoupling capacitor and an optional bulk capacitor depending on the application. Since the input current to the step-down converter is discontinuous, a capacitor is required to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed to the  $V_{IN}$  as close as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current is estimated with Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at  $V_{IN} = 2V_{OUT}$ , shown in Equation (5):

$$I_{CIN} = \frac{1}{2} \times I_{OUT} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple is estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

The worst-case condition occurs at  $V_{IN} = 2V_{OUT}$ , shown in Equation (7):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (7)$$

A ceramic capacitor over 10  $\mu\text{F}$  is recommended for the decoupling capacitor. An additional 0.1  $\mu\text{F}$  capacitor from the VIN pin to the ground is optional to provide additional high frequency filtering.

### Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple is estimated with Equation (8):

$$\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{F_{\text{SW}} \times L} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right) \times \left(R_{\text{ESR}} + \frac{1}{8 \times F_{\text{SW}} \times C_{\text{OUT}}}\right) \quad (8)$$

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple is estimated with Equation (9):

$$\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{8 \times F_{\text{SW}}^2 \times L \times C_{\text{OUT}}} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right) \quad (9)$$

For POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple is approximated with Equation (10):

$$\Delta V_{\text{OUT}} = \frac{V_{\text{OUT}}}{F_{\text{SW}} \times L} \times \left(1 - \frac{V_{\text{OUT}}}{V_{\text{IN}}}\right) \times R_{\text{ESR}} \quad (10)$$

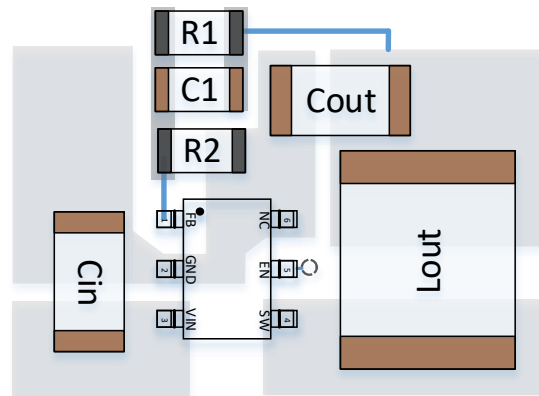
### PC Board Layout Considerations

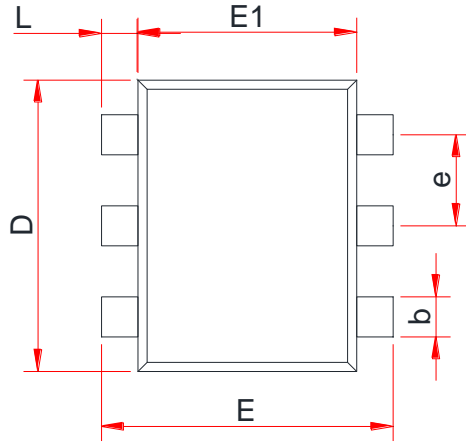
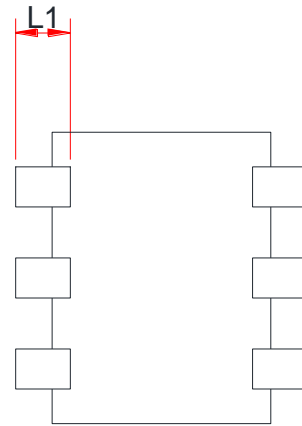
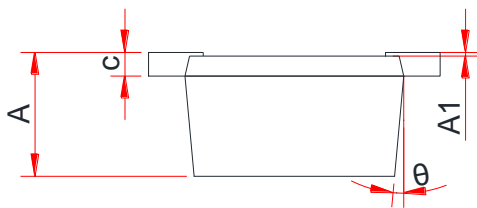
A good circuit board layout aids in extracting the most performance from the WD1072. Poor circuit layout degrades the output ripple and EMI or EMC performance.

The evaluation board layout is optimized for the WD1072. Use the layout for best performance. If the layout needs changing, follow the guidelines below:

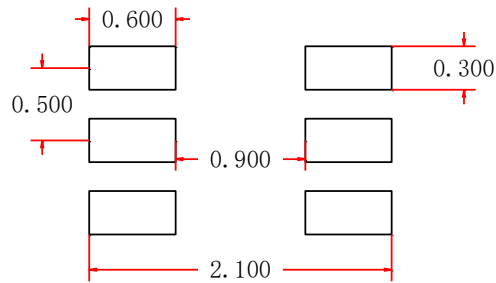
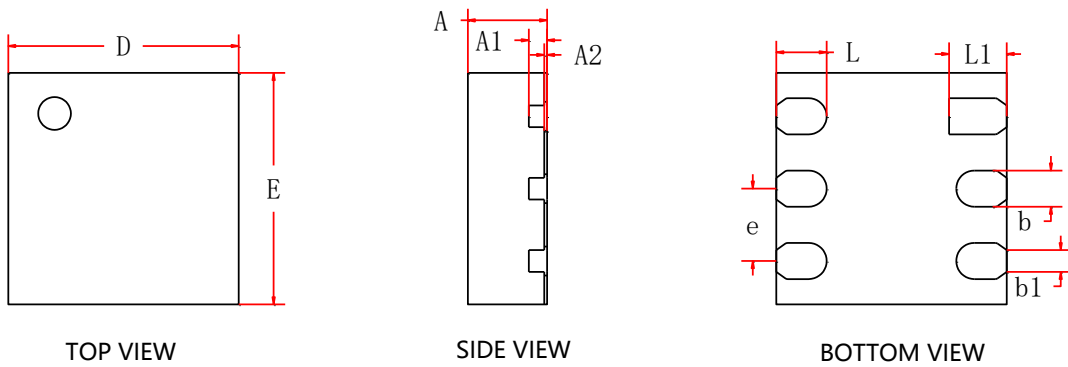
- Use wide and short traces for power paths (such as the VIN, the SW, and the GND) to improve efficiency and reduce parasitic inductance.
- The input low-ESR ceramic capacitor needs to be connected to the VIN and the GND pin as close as possible to the IC.

- Arrange a quiet path for output voltage sense and feedback network, and make it surrounded by a ground plane if possible. Place feedback network close to the IC.
- GND trace that connects the Cin, the GND pin, the NC pin, and the Cout should be as short and wide as possible to minimize the trace impedance. Big GND plane or layer is strongly recommended to improve thermal and noise performance.



**Package Outline Dimensions**
**SOT-563**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.45	0.52	0.60
A1	0.00	—	0.05
e	0.50BSC		
c	0.09	—	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.10	—	1.45
b	0.17	0.22	0.27
L	0.15Ref		
L1	0.25Ref		
$\theta$	7° Ref		

**DFN1616**


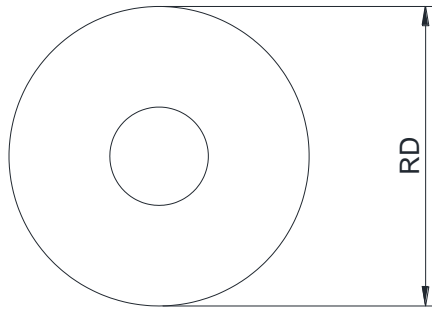
RECOMMENDED LAND PATTERN(Unit:mm)

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1		0.127 Ref.	
A2	0.00	0.02	0.05
D	1.50	1.60	1.70
E	1.50	1.60	1.70
b	0.20	0.25	0.30
b 1	0.10	0.15	0.20
e	0.50 BSC		
L	0.30	0.35	0.40
L1	0.35	0.40	0.45

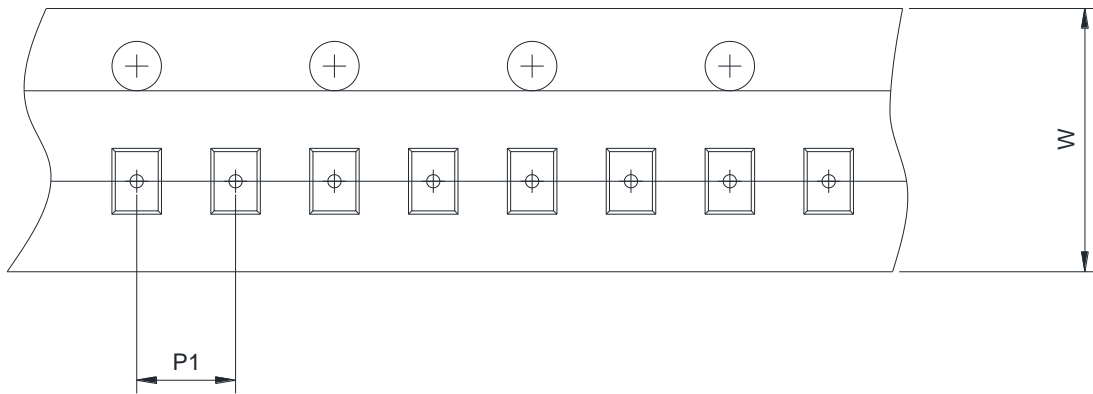


**Tape and Reel Information**

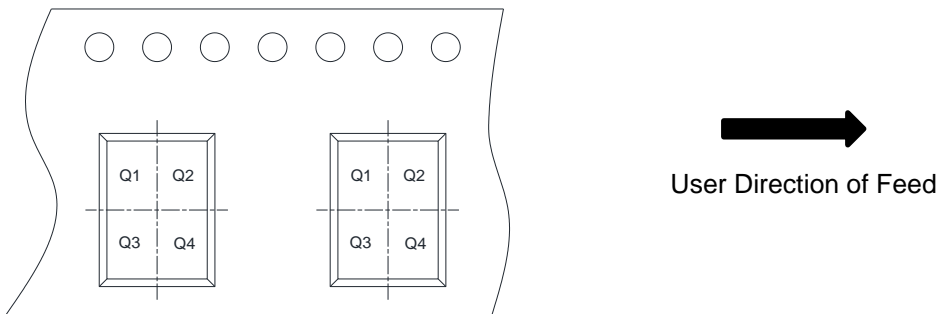
**Reel Dimensions**



**Tape Dimensions**



**Quadrant Assignments for PIN1 Orientation in Tape**



RD	Reel dimension	<input checked="" type="checkbox"/> 7inch	<input type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input checked="" type="checkbox"/> 8mm	<input type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input checked="" type="checkbox"/> 4mm <input type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input type="checkbox"/> Q1	<input type="checkbox"/> Q2 <input checked="" type="checkbox"/> Q3 <input type="checkbox"/> Q4