WL2863D

Ultra-Low Noise, High PSRR LDO, 250mA Linear Regulator for RF and Analog Circuits

Http://www.ovt.com

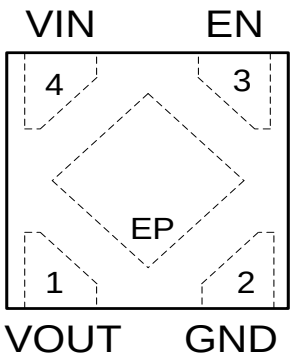
Descriptions

The WL2863D is a linear regulator capable of supplying 250-mA output current. Designed to meet the requirements of RF and analog circuits, the WL2863D device provides low noise, high PSRR, low quiescent current and very good load /line transients.

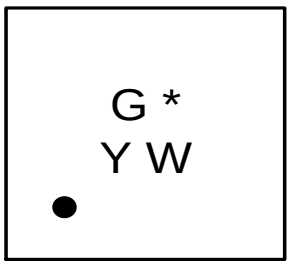
The device is designed to work with a 1μF input and 1μF output ceramic capacitor (no separate noise Operation bypass capacitor is required).

The WL2863D regulators are available in standard DFN1x1-4L Package. Standard products are Pb-free and Halogen-free.

DFN1X1-4L



Pin Configuration (Top View)



Marking
G : Device Code
*** : Voltage Code**
Y : Year Code
W: Week Codes

Features

- Input Voltage Range :2.2V~5.5V
- Output Voltage Range :1.2V~4.3V
- Output current :250mA
- PSRR :Typ.100dB at 10mA , f =1KHz
  :Typ. 45dB at 10mA , f =1MHz
- Low Dropout :Typ. 100mV at 250mA
- Quiescent current :Typ. 21μA
- Low Output Voltage Noise :Typ. 4.8μVRMS
- Output Voltage Tolerance :±1.5%
- Shutdown Current :Typ. 0.01μA
- UVLO Threshold(V) :Typ. 1.90V
- Recommend capacitor :1uF
- Stable with 1μF Ceramic Input and Output capacitor
- No Noise Bypass Capacitor Required
- Thermal-Overload Protection

Applications

- Cell phones , radiophone, digital cameras
- Bluetooth, wireless handsets
- Hifi products
- Others portable electronics device

Order Information

For detail order information, please see page 8

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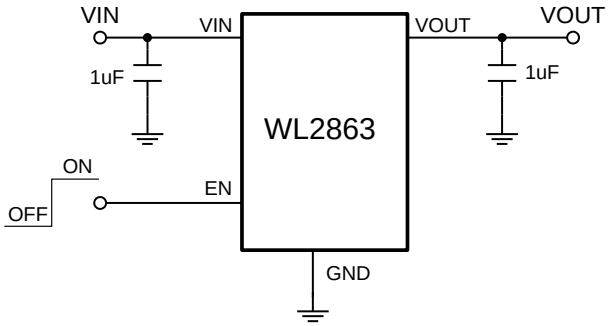
Typical Application

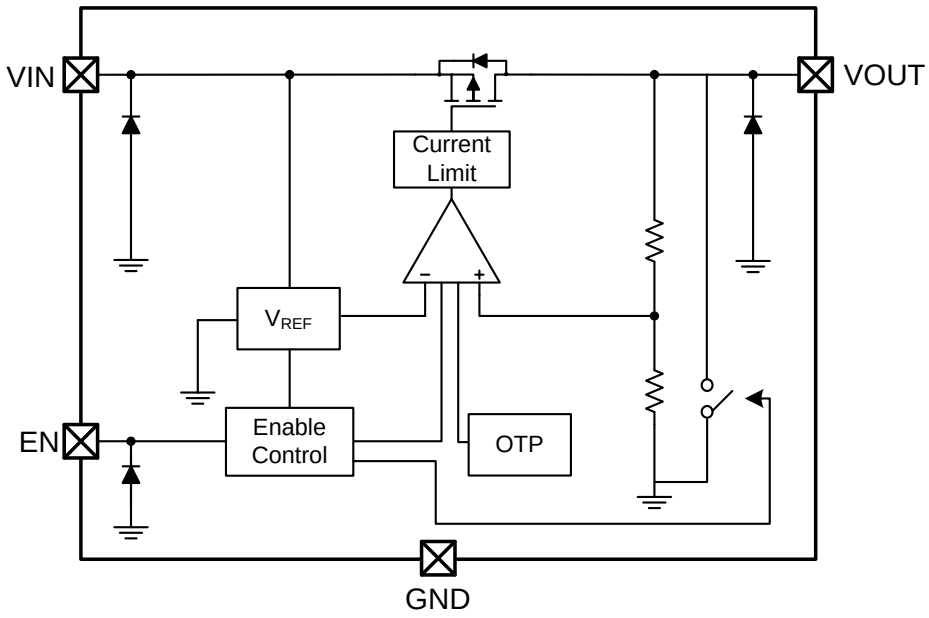


Note : The input and output capacitor must be located a distance of not more than 1 cm

PIN Functions

PIN	Symbol	Description
1	VOUT	Regulated output voltage. 1μF capacitor should be connected at this input
2	GND	Common ground connection
3	EN	Chip enable: Applying VEN < 0.4 V disables the regulator, Pulling VEN > 1.2 V enables the LDO.
4	VIN	Input voltage supply pin , 1μF capacitor should be connected at this input
EP		Expose pad can be tied to ground plane for better power dissipation

Block Diagram



Absolute Maximum Ratings

Parameter		Value	Unit
Power Dissipation, P_D@T_A=25℃		Internally Limited	mW
V_{IN} Range		-0.3～6.0	V
V_{EN} Range		−0.3 to V_{IN} + 0.3	V
V_{OUT} Range		−0.3 to V_{IN} + 0.3	V
I_{OUT}		250	mA
Lead Temperature Range		260	°C
Storage Temperature Range		-55 ~ 150	°C
Operating Junction Temperature Range		150	°C
ESD Ratings	HBM	2000	V
	MM	200	V

Recommend Operating Ratings

Parameter	Value	Unit
Operating Supply voltage	2.2～5.5	V
Operating Temperature Range	-40～85	°C
Thermal Resistance, $R_{\theta JA}$	250	°C/W

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Electronics Characteristics (V_{IN}=$V_{OUT(NOM)}$+1V, C_{IN}=C_{OUT}=1uF, V_{EN} = 1.2 V. Typical values are at Ta = +25°C ,unless otherwise noted)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Input Voltage	V_{IN}		2.2		5.5	V
Output Voltage Accuracy	V_{OUT}	V_{IN} = $V_{OUT(NOM)}$ + 1 V I_{OUT}=1mA	-1.5		+1.5	%
Output Current Limit	I_{LIM}	VOUT = 90% VOUT(NOM)	250			mA
Dropout Voltage		V_{OUT}=2.8$V_{(NOM)}$, I_{OUT}=250mA		100	170	mV
		V_{OUT}=3.0$V_{(NOM)}$, I_{OUT}=250mA		98	162	
		V_{OUT}=3.3$V_{(NOM)}$, I_{OUT}=250mA		92	150	
Line Regulation	△V_{LINE}	V_{IN}=2.2V~5V ,I_{OUT}=1mA		0.1		mV
Load Regulation	△V_{Load}	I_{OUT}=1~200mA		15		mV
Quiescent Current	I_Q	I_{OUT}=0mA		21	25	μA
Short Current	I_{SHORT}	V_{OUT}=0V		350		mA
Shut-down Current	I_{SHDN}	V_{EN} <0.4 V, V_{IN} = 4.8 V		0.01	1.0	μA
Power Supply Rejection Rate	PSRR	I_{OUT} =10mA, f=100Hz		90		dB
		I_{OUT} =10mA, f=1KHz		100		
		I_{OUT} =10mA, f=100KHz		60		
		I_{OUT} =10mA, f=1MHz		45		
EN logic high voltage	V_{ENH}	V_{IN}=5.5V, I_{OUT}=1mA	1.2			V
EN logic low voltage	V_{ENL}	V_{IN}=5.5V, V_{OUT}=0V			0.4	V
EN Input Current	I_{EN}	V_{EN} = 0 to 5.5V			1	μA
Turn−On Time		C_{OUT} = 1μF, From assertion of V_{EN} to V_{OUT} = 95% $V_{OUT\ (NOM)}$		1.5		mS
Output Voltage Noise	e_{NO}	10Hz to 100KHz, I_{OUT} =1mA		7		μVRMS
		10Hz to 100KHz, I_{OUT} =200mA		4.8		
Thermal shutdown threshold	T_{SDH}	Temperature rising		150		°C
	T_{SDL}	Temperature falling		120		°C
Under voltage lock out threshold	V_{UVLO}			1.9		V
Active Output Discharge Resistance	R_{LOW}	V_{EN}<0.4V		300		Ω
Line Transient	$Tran_{LINE}$	V_{IN} = ($V_{OUT(NOM)}$ + 2 V) to ($V_{OUT(NOM)}$ + 1 V) in 30 us, I_{OUT} = 1 mA	−1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 2 V) in 30 us, I_{OUT} = 1 mA			+1	
Load Transient	$Tran_{LOAD}$	I_{OUT} = 1 mA to 200 mA in 10 us	−10			mV
		I_{OUT} = 200 mA to 1 mA in 10 us			+10	

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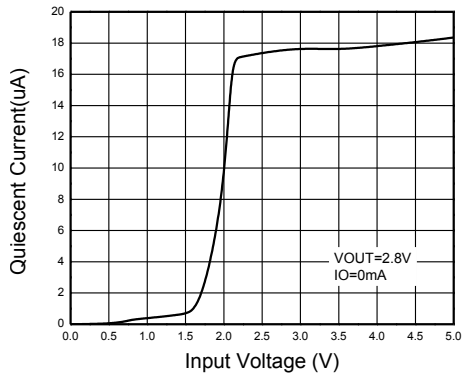
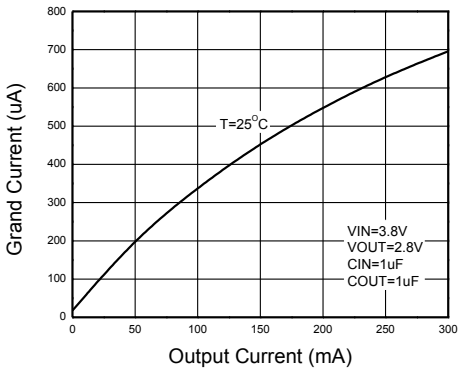
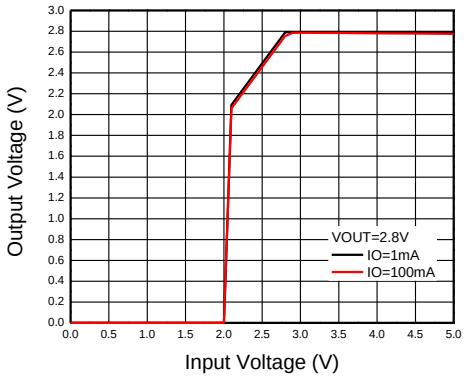
Typical characteristics (Ta=25 °C, V_{IN}=3.8V, V_{OUT} = 2.8V C_{IN}=C_{OUT}=1uF, unless otherwise noted)



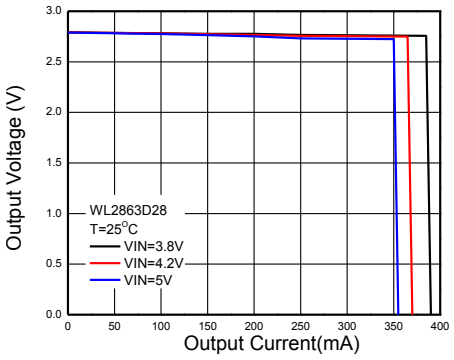
Quiescent current vs. Supply voltage



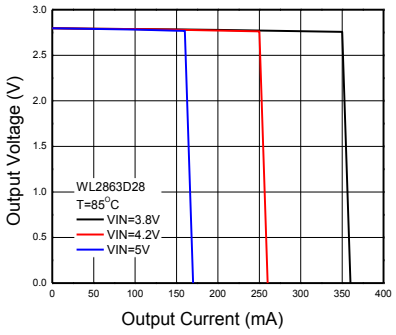
Ground Current vs. Load Current



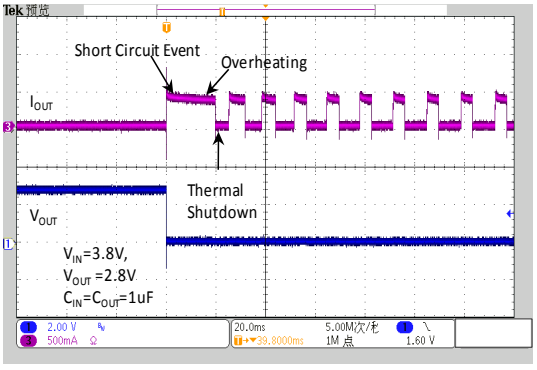
Output voltage vs. Supply voltage



Output voltage vs. Output current



Output voltage vs. Output current



Short Circuit and Thermal Shutdown

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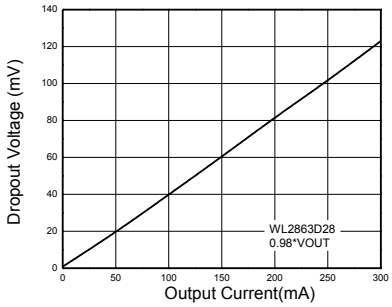
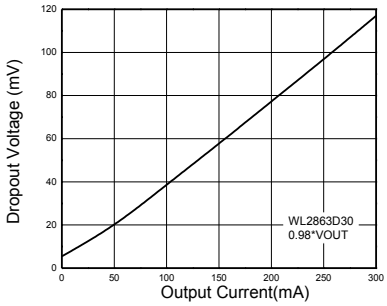
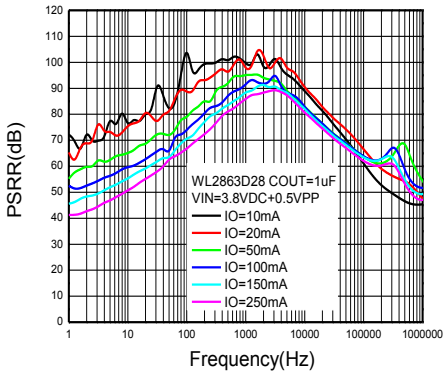


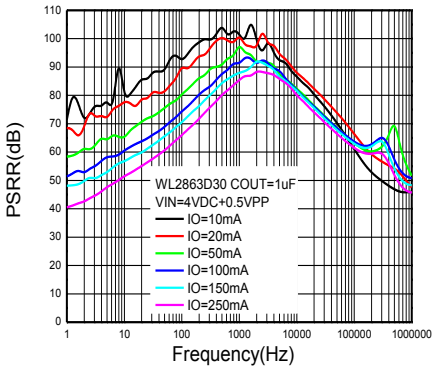
Dropout Voltage vs. Output Current



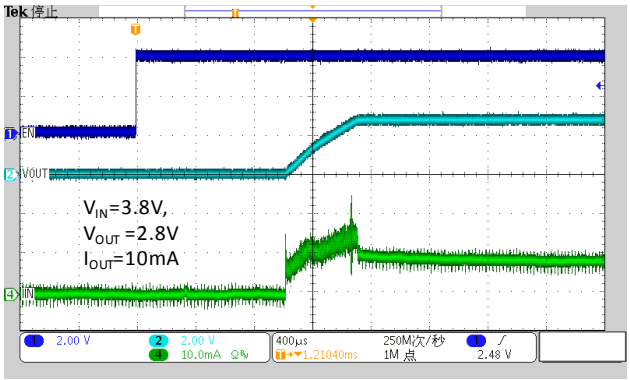
Dropout Voltage vs. Output Current



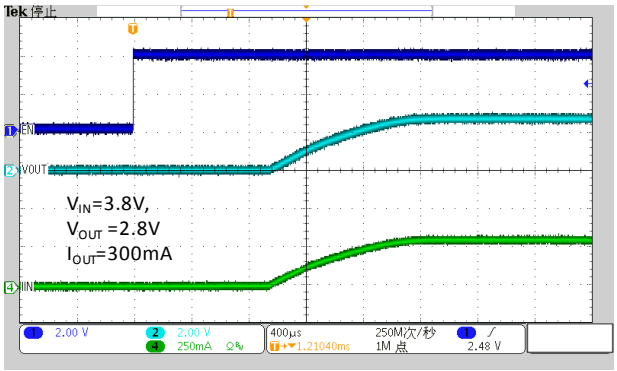
PSRR



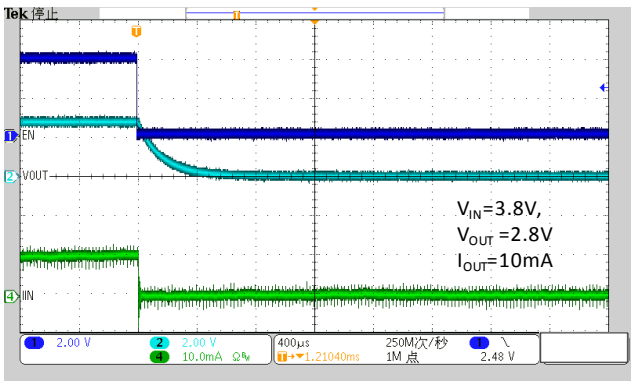
PSRR



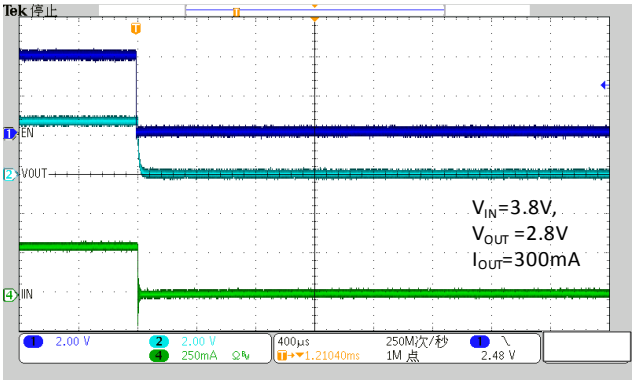
Soft-Start From EN



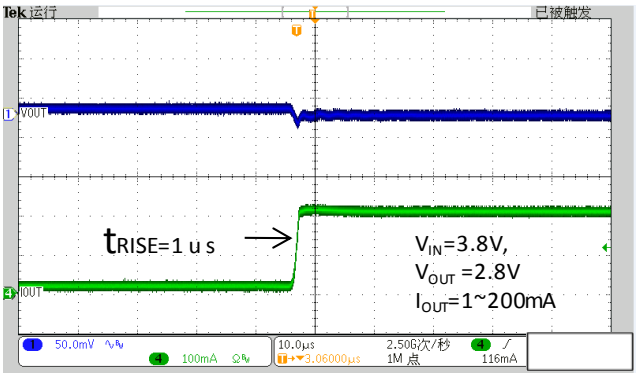
Soft-Start From EN



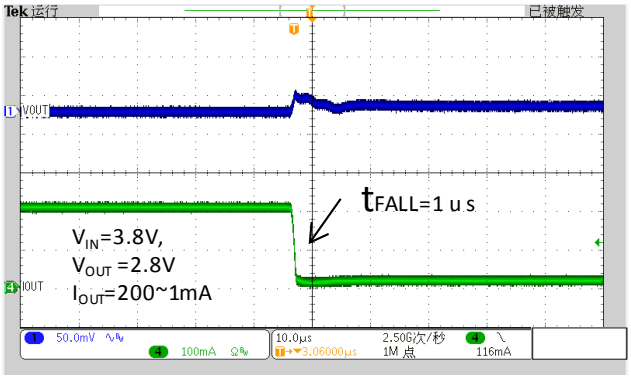
EN Shutdown



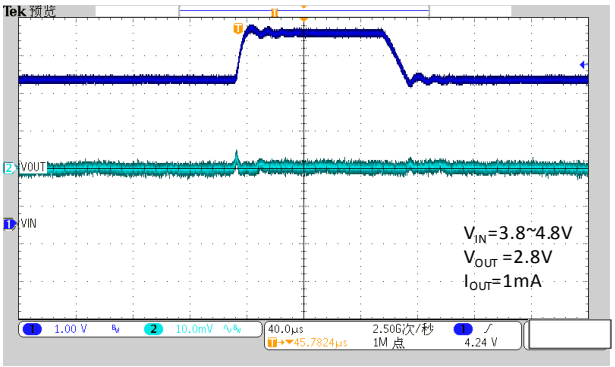
EN Shutdown



Load Transient Response



Load Transient Response



Line Transient Response

ORDER INFORMATION

Ordering No.	Vout (V)	Package	Operating Temperature	Marking	Shipping
WL2863D18-4/TR	1.8	DFN1x1-4L	-40~+85°C	GH YW	Tape and Reel, 10000
WL2863D25-4/TR	2.5	DFN1x1-4L	-40~+85°C	GK YW	Tape and Reel, 10000
WL2863D28-4/TR	2.8	DFN1x1-4L	-40~+85°C	GL YW	Tape and Reel, 10000
WL2863D285-4/TR	2.85	DFN1x1-4L	-40~+85°C	GV YW	Tape and Reel, 10000
WL2863D30-4/TR	3.0	DFN1x1-4L	-40~+85°C	GM YW	Tape and Reel, 10000
WL2863D33-4/TR	3.3	DFN1x1-4L	-40~+85°C	GN YW	Tape and Reel, 10000
WL2863D36-4/TR	3.6	DFN1x1-4L	-40~+85°C	Gf YW	Tape and Reel, 10000

Marking:

G* = Device Code
Y = Year
W = Week

PACKAGE OUTLINE DIMENSIONS

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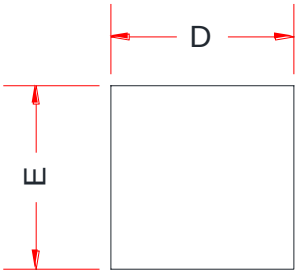
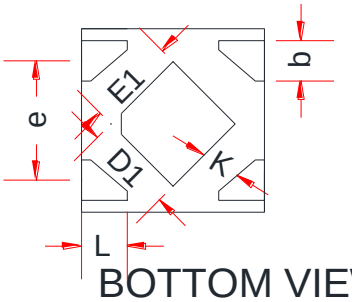
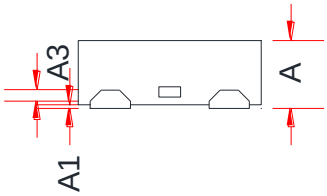
DFN1x1-4L



TOP VIEW



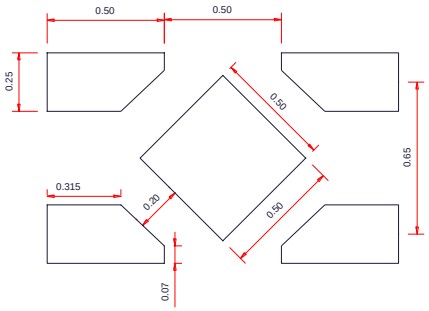
BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.34	0.37	0.40
A1	0.00	0.02	0.05
A3	0.10 Ref.		
b	0.17	0.22	0.28
L	0.17	-	0.33
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D1	0.43	0.48	0.53
E1	0.43	0.48	0.53
e	0.65BSC		
K	0.22Ref.		

Recommend PCB Layout (Unit: mm)



Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

TAPE AND REEL INFORMATION

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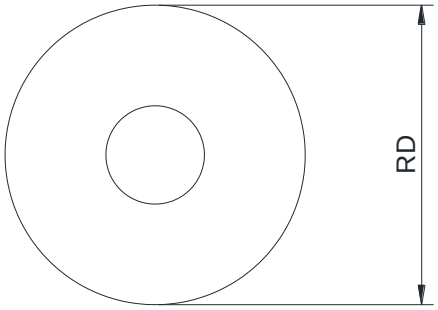
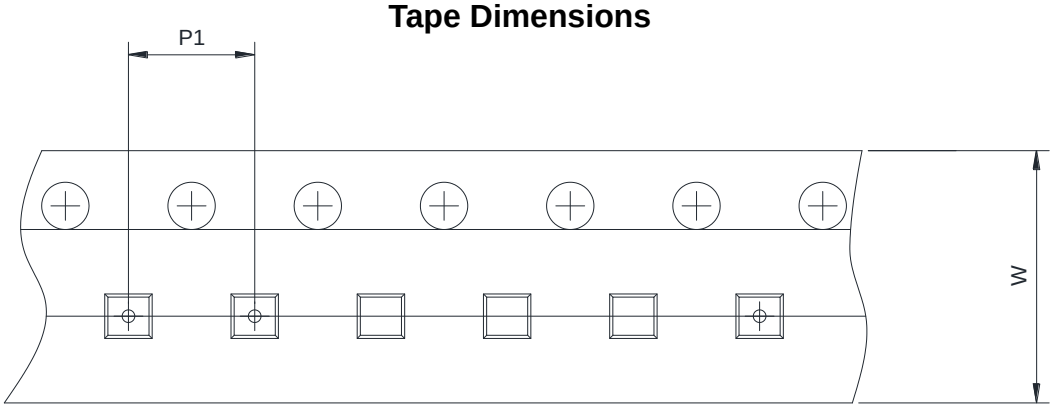
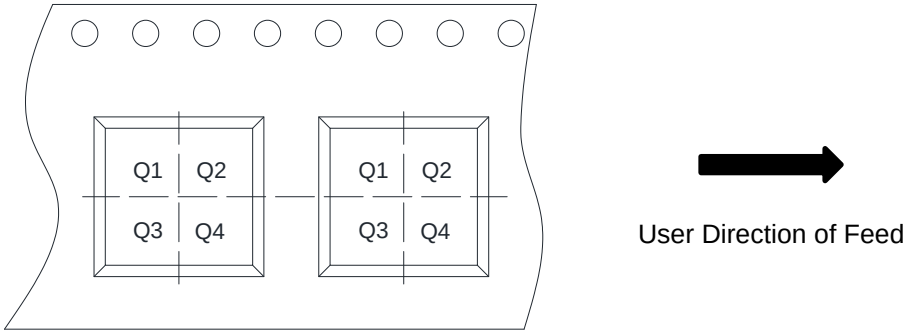
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☑ 2mm	☐ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4

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