WD3102C

Dual Output AMOLED Bias

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Descriptions

The WD3102 is a highly integrated Boost, LDO and inverting charge pump to generate positive and negative output voltage. The negative output voltages can be adjusted from -0.6V to -2.4V with 100mV steps by SWIRE interface protocol. The part maintains the highest efficiency by utilizing a -0.33x/-0.5x mode fractional charge pump with automatic mode transition. With its input voltage range of 2.5V to 4.6V, WD3102 is optimized for products powered by single-cell battery and the output current up to 30mA.

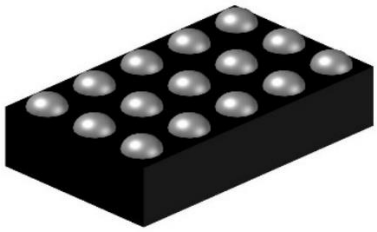
The WD3102C is available in CSP-15L package. Standard products is Pb-Free and Halogen-Free.

Features

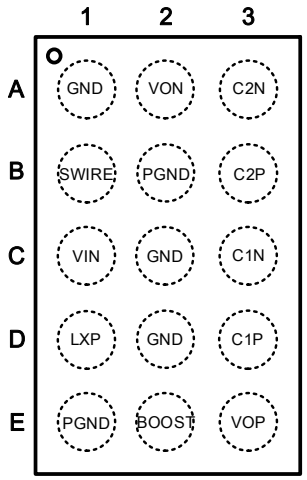
- 2.5V to 4.6V Supply Voltage Range
- Shutdown Current < 1μA
- Single Wire Protocol
- Fixed 4.6V Positive Voltage Output
- Negative Voltage Output from -0.6V to -2.4V per 0.1V by SWIRE Pin
- Auto-Mode Transition of -0.33x/-0.5x Charge Pump
- Built-in Soft-Start
- 40mA Maximum Output Current
- Programmable Output Fast Discharge Function
- High Impedance Output when IC Shutdown
- UVLO, OCP, SCP, OTP, OVP Protection

Applications

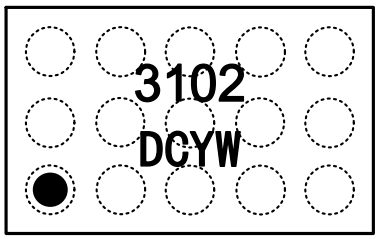
- AMOLED Bias in Portable Device



CSP-15L Package



Pin configuration (Top view)



3102 = Device code
DC =Special Code
Y = Year code
W = Week code

Marking

Order information

Device	Package	Shipping
WD3102C-15/TR	CSP-15L	3000/Reel&Tape

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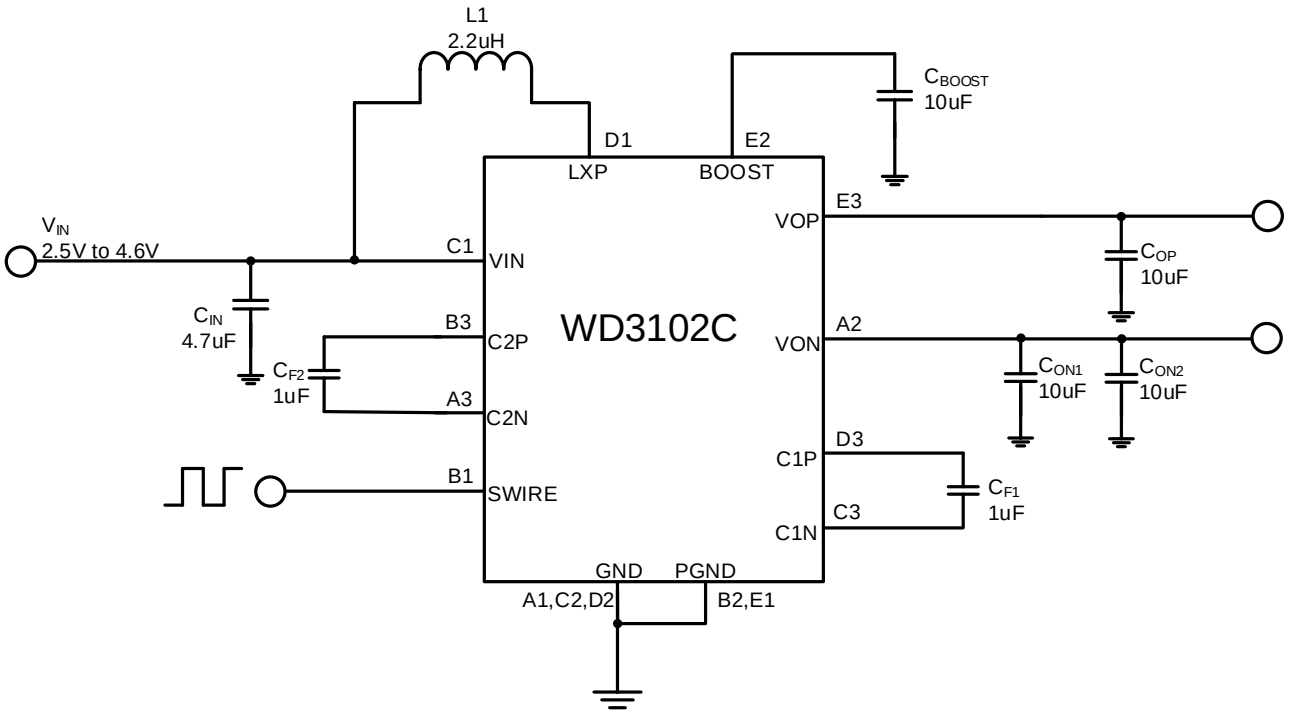
Typical Applications



Pin Descriptions

Symbol	Pin Number	Descriptions
GND	A1, C2, D2	Ground.
VON	A2	Negative Terminal Output.
C2N	A3	Flying Capacitor 2 Negative Connection.
SWIRE	B1	Enable and VON Voltage Setting.
PGND	B2, E1	Power Ground.
C2P	B3	Flying Capacitor 2 Positive Connection.
VIN	C1	Power Input.
C1N	C3	Flying Capacitor 1 Negative Connection.
LXP	D1	Switching Node of Boost Converter.
C1P	D3	Flying Capacitor 1 Positive Connection.
BOOST	E2	Output Voltage of Boost Converter.
VOP	E3	Positive Terminal Output.

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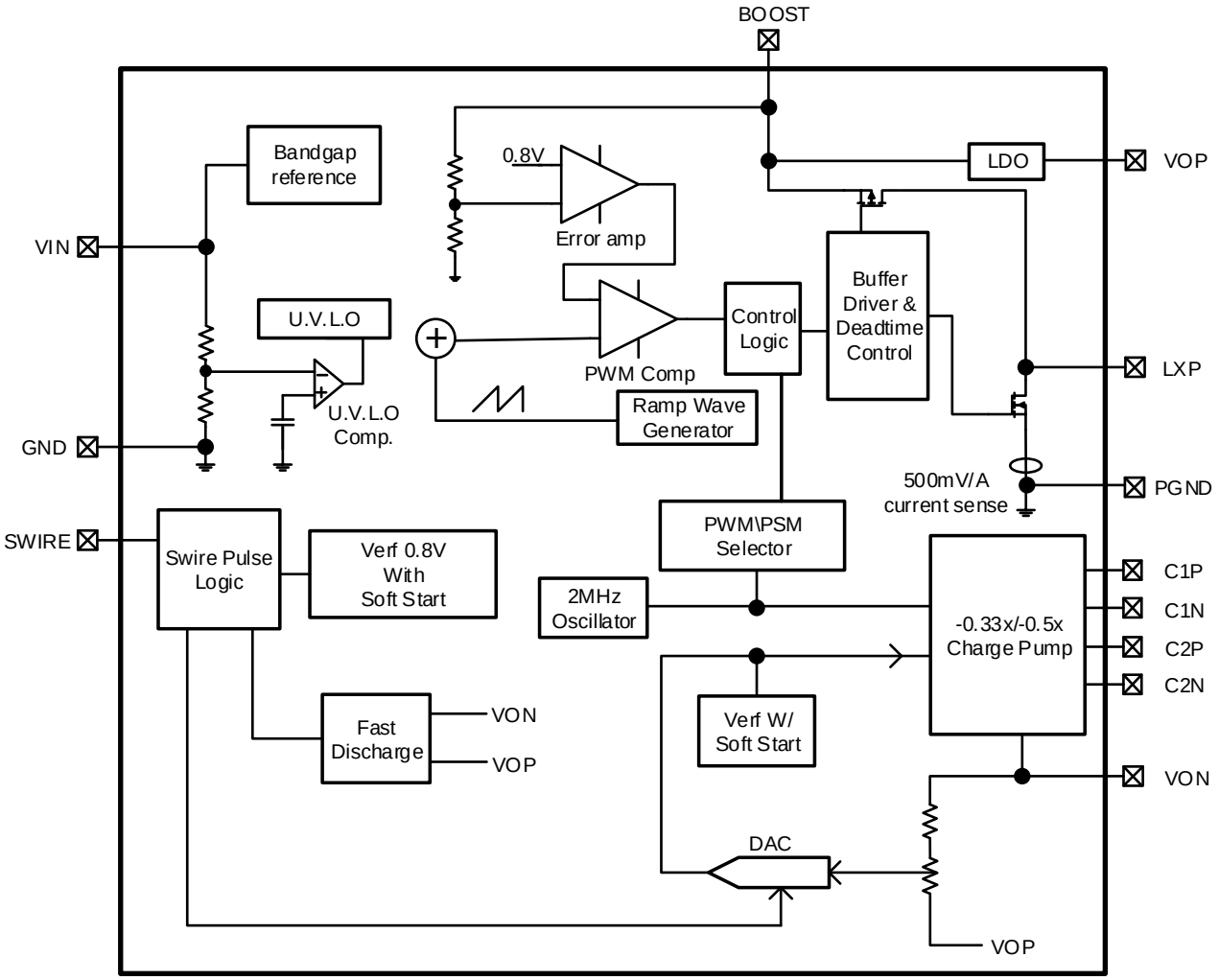
Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
VIN pin voltage range	V_{IN}	-0.3～+6	V
Output pin VOP voltage range	-	-0.3～+6	V
Output pin VON voltage range	-	-6～0.3	V
LXP pin voltage range (DC)	V_{SW}	-0.3～+6	V
All Other Pins Voltage	-	-0.3~ +6	V
Power Dissipation – CSP-15L (Note 1)	P_D	2	W
Thermal Characteristics (Note 1)	$R_{\theta JA}$	49.8	°C/W
	$R_{\theta JC}$	32	°C/W
Maximum Junction Temperature	T_J	150	°C
Lead temperature(Soldering, 10s)	T_L	260	°C
Storage temperature	Tstg	-65 ~ 150	°C
ESD Classification	HBM		V
	CDM		V

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These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Note 1: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 125°C (typ.).

Note 2: Junction-to-ambient thermal resistance ($R_{\theta JA}$) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7.

Recommended Operating Conditions

Parameter	Symbol	MIN	NOM	MAX	Unit
Supply input voltage range	V_I	2.5		4.6	V
Positive Output Voltage	V_{OP}		4.6		V
Negative Output Voltage Range	V_{ON}	– 2.4		– 0.6	V
Ambient Temperature Range	Topr	– 40		85	ºC
Junction Temperature Range	T_J	– 40		125	ºC

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Electronics Characteristics

(V_{IN} = 3.7V, V_{OP} = 4.6V, V_{ON} = -2.4V, C_{IN} = 4.7µF, C_{BOOST} = C_{OP} = 10µF, C_{ON} = 20µF, C_{F1} = 1µF, L1 = 2.2µH, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Power Supply						
Input Voltage Range	V_{IN}		2.5		4.6	V
V_{IN} Under Voltage Lockout Threshold	V_{UVLO}	Rising		2.2	2.5	V
		Falling		2.1	2.3	
Shutdown Supply Current	I_{SHDN}	Swire = 0 V		--	1	uA
Over Temperature Protection	T_{OTP}			150		°C
OTP Hysteresis				20		°C
Efficiency Peak 1	Eff_1	I_{OP} = I_{ON} = 1 mA		63		%
Efficiency Peak 2	Eff_2	I_{OP} = I_{ON} = 5 mA		81		%
Efficiency Peak 3	Eff_3	I_{OP} = I_{ON} = 15 mA		86		%
LDO Output						
Positive Output Voltage Range	V_{OP}			4.6		V
Positive Output Voltage Accuracy	V_{OP_ACC}		-1		1	%
Positive Output Current Capability	I_{OP_MAX}				40	mA
Positive Output Voltage Ripple	V_{OP_RIPPLE}	I_{OP} = 20 mA		10		mV
Line Regulation	Δ_{LINE}	V_{IN} = 2.9V to 4.5V, I_{OP} = 20 mA		5		mV
Load Regulation	Δ_{LOAD}	I_{OP} = 0 mA to 20 mA		5		mV
Fast Discharge Resistance	R_{DISP}			105		Ω
Short Circuit Protection	V_{SCP1}			<80%V_{OP}		V
Negative Charge Pump Output						
Negative Output Voltage Range	V_{ON}		-2.4		-0.6	V
Negative Output Voltage Setting Range	V_{ON_SET}			100		mV
Negative Output Voltage Accuracy	V_{ON_ACC}		-1		1	%
Negative Output Current Capability					40	mA
Negative Output Voltage Ripple	V_{ON_RIPPLE}	I_{OP} = 20 mA		20		mV
Line Regulation	V_{ON_LINE}	V_{IN} = 2.9 to 4.5V, I_{on} = 20 mA		5		mV
Load Regulation	V_{ON_LOAD}	I_{ON} = 0 mA to 30 mA		10		mV
Negative Charge Pump Switching Frequency	f_{OSC_N}		0.8	1	1.2	MHz

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Electronics Characteristics(Continued)

(V_{IN} = 3.7V, V_{OP} = 4.6V, V_{ON} = -2.4V, C_{IN} = 4.7μF, C_{BOOST} = C_{OP} = 10μF, C_{ON} = 20μF, C_{F1} = 1μF, L1 = 2.2μH, T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Negative Charge Pump Output						
Fast Discharge Resistance	R_{DISN}			60		Ω
Short Circuit Protection	V_{SCP2}			>80%V_{ON}		V
Logic Input (SWIRE)						
SWIRE Turn-off Detection Time	T_{off_dly}		350			μS
SWIRE Signal Stop Indicate Time	T_{stop}		350			μS
Twait after Data	T_{wait_int}		10			mS
Rising Input High Threshold	V_{IH}		1.2		V_{IN}	V
Falling Input Low Threshold	V_{IL}		-		0.4	V
SWIRE Pull Low Resistor	R_{SWIRE}			300		kΩ
Wake up Delay	T_{wkp}				1	μS
SWIRE Rising Time	T_R				200	nS
SWIRE Falling Time	T_F				200	nS
Clocked SWIRE High	T_{ON}		2	10	40	uS
Clocked SWIRE Low	T_{OFF}		2	10	40	uS
SWIRE to VOP On Time	T_{ON}			1.6		mS
Input Clocked SWIRE Frequency	F_{SWIRE}		25		250	kHz

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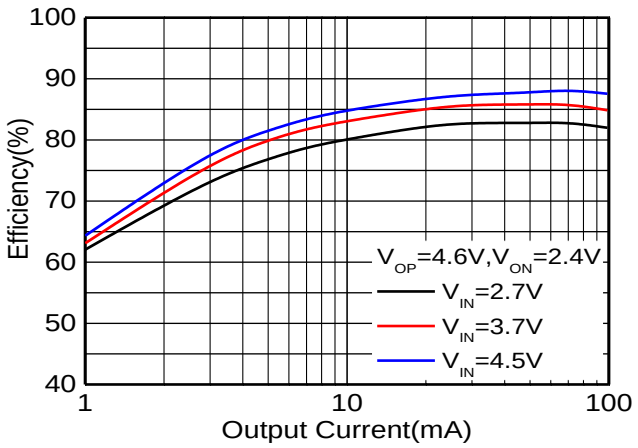
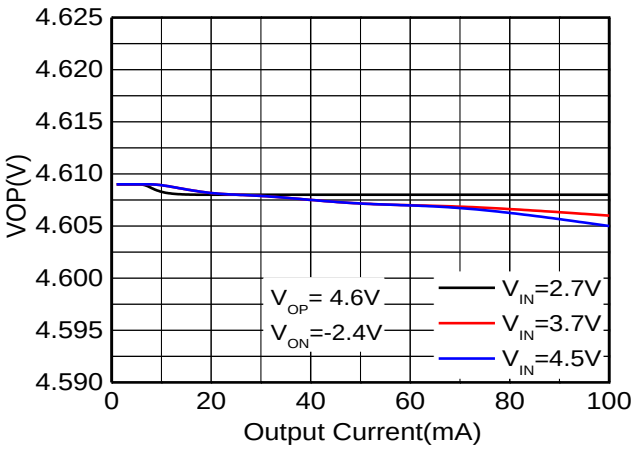
Typical Characteristics

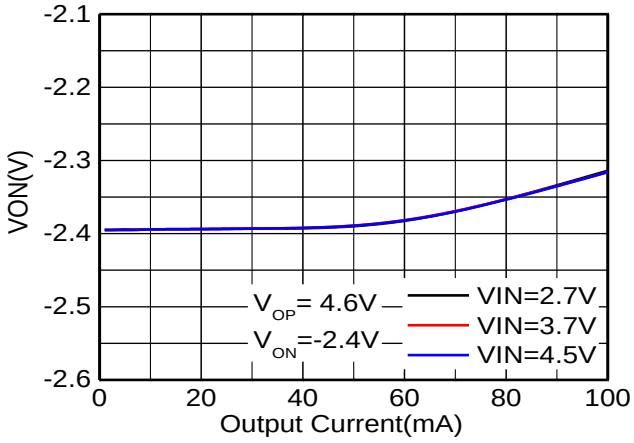
(Ta=25°C, V_{IN}=3.7V, V_{OP}=4.6V, V_{ON}=-2.4V, C_{IN}=4.7uF, C_{BOOST}=C_{OP}=10uF, C_{ON}=20uF, C_{F1}= C_{F2}=1uF, L1=2.2uH, unless otherwise noted)



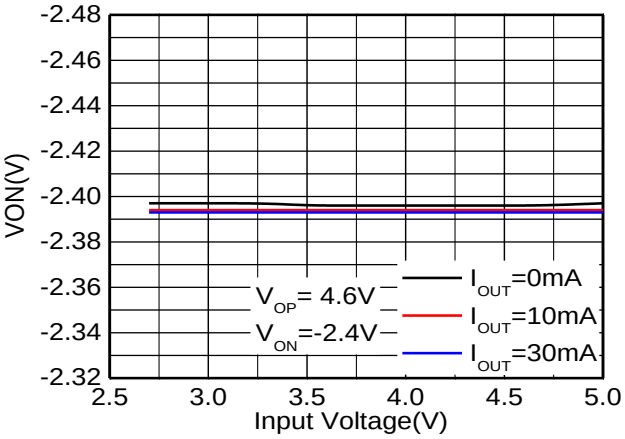
Efficiency vs. Output Current



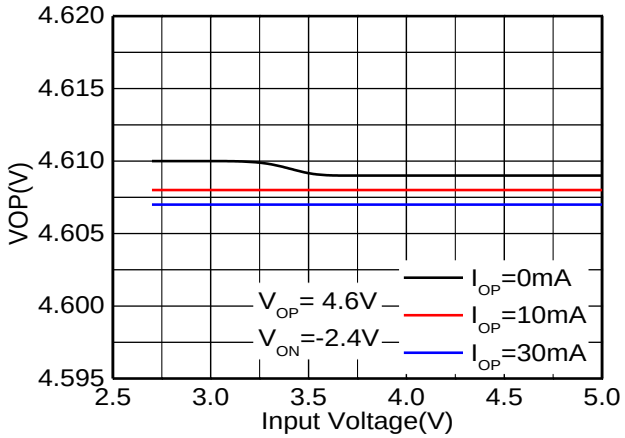
V_{OP} vs. Output Current



V_{ON} vs. Output Current



V_{ON} vs. Input Voltage



V_{OP} vs. Input Voltage

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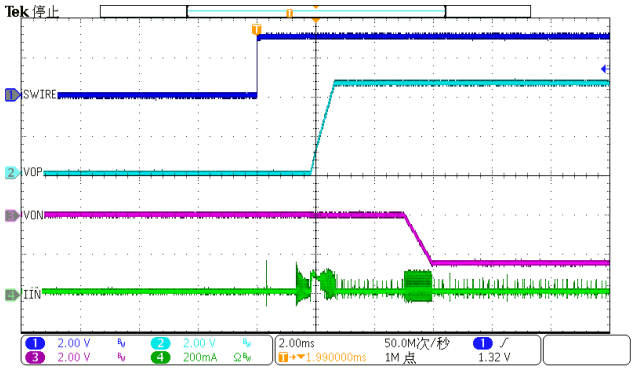
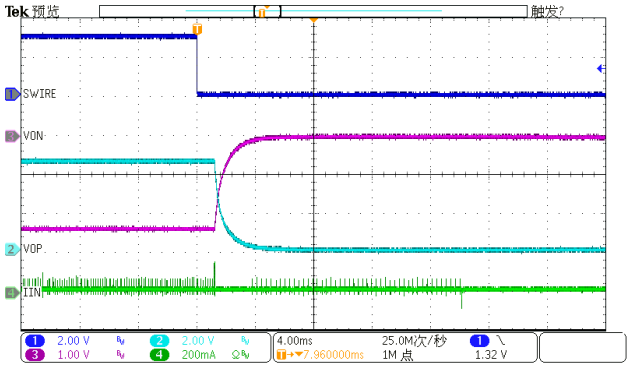
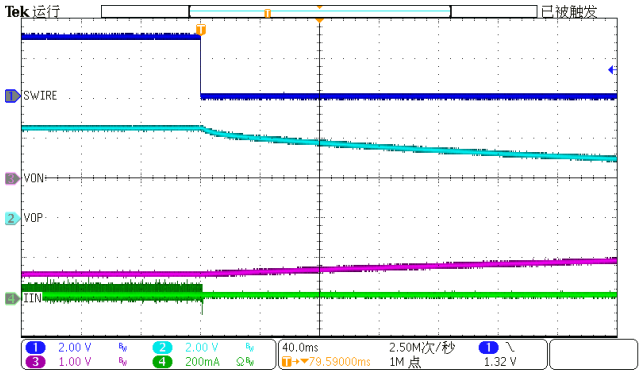


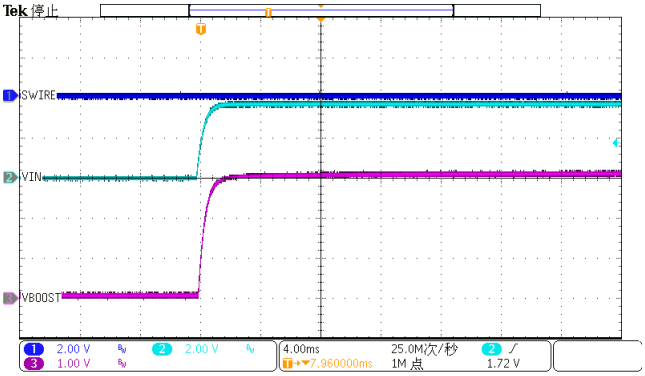
SWIRE On



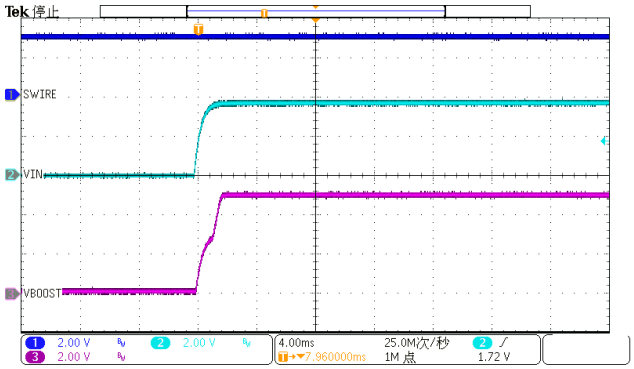
SWIRE OFF with Discharge



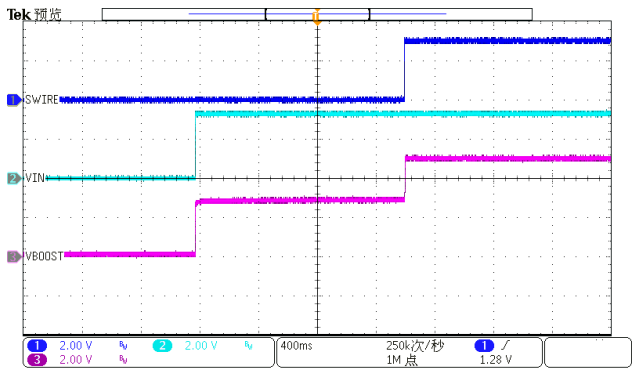
SWIRE OFF without Discharge



Power On with SWIRE is Low



Power On with SWIRE is High



Power On with SWIRE from Low to High

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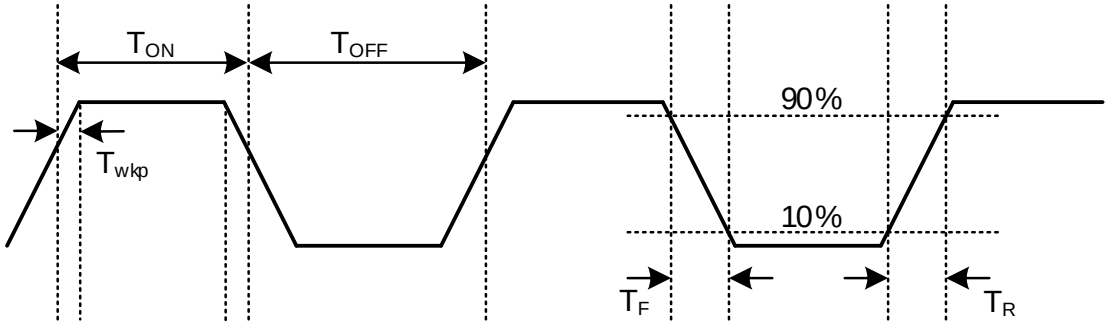
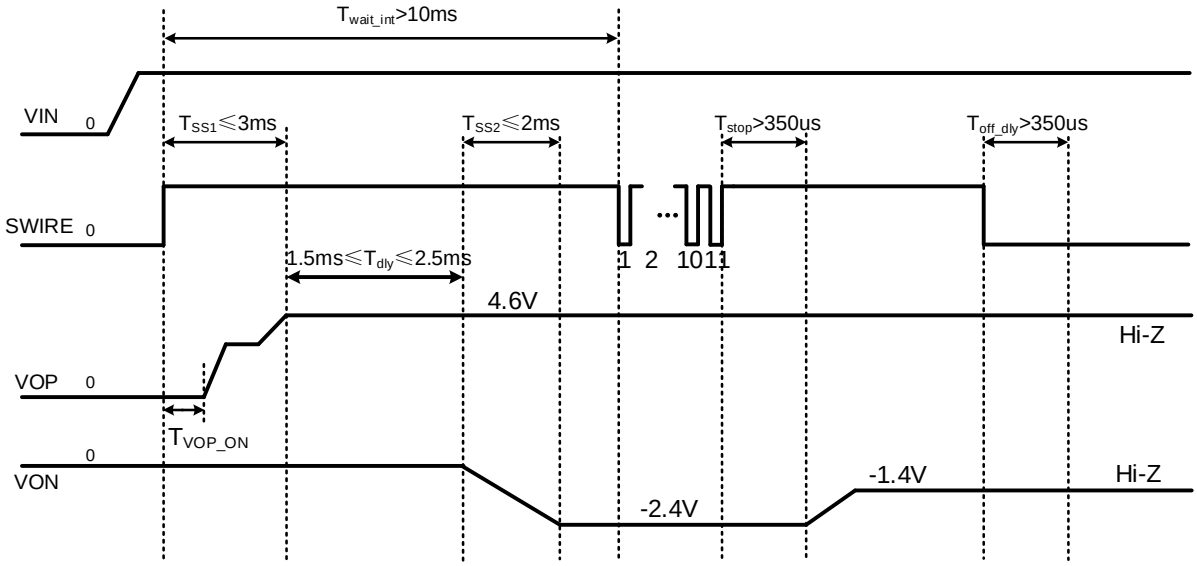
Time Diagram

SWIRE Interface



Power Sequence



Pluse	VON(V)
0	-2.4(default)
1	-2.4
2	-2.3
3	-2.2
4	-2.1
5	-2.0
6	-1.9
7	-1.8
8	-1.7
9	-1.6
10	-1.5
11	-1.4
12	-1.3
13	-1.2
14	-1.1
15	-1.0
16	-0.9
17	-0.8
18	-0.7
19	-0.9
20	0

VON Output Voltage with SWIRE Pulse

Pluse	VON(V)
21	Enable

VOP/VON Shutdown Discharge Selection with SWIRE Pulse

Once pulse 21 received on SWIRE pin, the WD3102C will enable the discharge function to discharge the VOP/VON outputs for 20ms and then enter high impedance state when fault or power-off condition. The discharge function is default disabled and outputs keep high impedance state when fault or power-off condition .

Operation Informations

The WD3102C is a highly integrated Boost, LDO and inverting charge pump to generate positive and negative output voltage. It can support input voltage range from 2.5V to 4.6V and the output current up to 30mA. The VOP positive output voltage is set at a typical value of 4.6V. The VON negative output voltage is set at a typical value of -2.4V and can be programmed through single wire protocol (SWIRE pin).

The available voltage range is from -0.6V to -2.4V with 100mV per step. The WD3102C provides Over- Temperature Protection (OTP) and Short Circuit Protection (SCP) mechanisms to prevent the device from damage with abnormal operations. When the SWIRE voltage is logic low for more than 350us, the IC will be shut down with low input supply current less than 1uA.

Application Informations

The WD3102C is a highly integrated Boost, LDO and inverting charge pump to generate positive and negative output voltages for AMLOED bias. It can support input voltage range from 2.5V to 4.6V and the output current up to 30mA. The VOP positive output voltage is generated from the LDO supplied from a synchronous Boost converter, and VOP is set at a typical value of 4.6V. The Boost converter output also drives an inverting charge pump controller to generate VON negative output voltage which is set at a typical value of -2.4V. The negative output voltage can be programmed through the dedicated pin which implements single wire protocol and the available voltage range is from -0.6V to -2.4V with 100mV per step.

Input Capacitor Selection

Input ceramic capacitor with 4.7uF capacitance is suggested for applications. For better voltage filtering, select ceramic capacitors with low ESR, X5R and X7R types are suitable because of their wider voltage and temperature ranges.

Boost Inductor Selection

The inductance depends on the maximum input current. As a general rule, the inductor ripple current range is 20% to 40% of the maximum input current. If 40% is selected as an example, the inductor ripple current can be calculated according to the following equations :

$$I_{IN(MAX)} = \frac{V_{OUT} \times I_{OUT(MAX)}}{V_{IN} \times \eta}$$

$$\Delta I_L = 0.4 \times I_{IN(MAX)}$$

where η is the efficiency of the VOP Boost converter, $I_{IN(MAX)}$ is the maximum input current, and ΔI_L is the inductor ripple current. The input peak current can then be obtained by adding the maximum input current with half of the inductor ripple current as shown in the following equation :

$$I_{PEAK} = 1.2 \times I_{IN(MAX)}$$

Note that the saturated current of the inductor must be greater than IPEAK.

The inductance can eventually be determined according to the following equation :

$$L = \frac{\eta \times (V_{IN})^2 \times (V_{OUT} - V_{IN})}{0.4 \times (V_{OUT})^2 \times I_{OUT(MAX)} \times f_{OSC}}$$

Where fOSC is the switching frequency. For better system performance, a shielded inductor is preferred to avoid EMI problems.

Boost Output Capacitor Selection

The output ripple voltage is an important index for estimating IC performance. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. ΔV_{OUT1} can be evaluated based on the ideal energy equalization. According to the definition of

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Q, the ΔV_{OUT1} value can be calculated as the following equation :

$$Q = I_{OUT} \times D \times \frac{1}{f_{OSC}} = C_{OUT} \times \Delta V_{OUT1}$$

$$\Delta V_{OUT1} = \frac{I_{OUT} \times D}{f_{OSC} \times C_{OUT}}$$

where f_{osc} is the switching frequency and D is the duty cycle.

Finally, taking ESR into consideration, the overall output ripple voltage can be determined by the following equation :

$$\Delta V_{OUT} = \Delta V_{ESR} + \Delta V_{OUT1} = \Delta V_{ESR} + \frac{I_{OUT} \times D}{f_{OSC} \times C_{OUT}}$$

where $\Delta V_{ESR} = I_{Crms} \times R_{CESR}$

The output capacitor, C_{OUT}, should be selected accordingly.

Under Voltage Lockout

To prevent abnormal operation of the IC in low voltage condition, an under voltage lockout is included which shuts down IC operation when input voltage is lower than the specified threshold voltage.

Soft-Start

The WD3102C employs an internal soft-start feature to avoid high inrush current during start-up. The soft-start function is achieved by clamping the output voltage of the internal error amplifier with another voltage source that is increased slowly from zero to near VIN during the soft-start period.

Negative Output Voltage Setting

The Negative output voltage can be programmed by a MCU through the dedicated pin according to Table "V_{ON} Output Voltage with SWIRE Pulse".

Shutdown Delay and Discharge

When the SWIRE signal is logic low for more than 350us, the IC function will be shut down. The output V_{OP}/V_{ON} can be actively discharged to GND with discharge function enabled referring to Table "VOP/VON Shutdown Discharge Selection with SWIRE Pulse". In shutdown mode, the input supply current for the IC is less than 1uA.

Over Current Protection

The WD3102C includes a cycle-by-cycle current limit function which monitors the inductor current during each ON period. The power switch will be forced off to avoid large current damage once the current is over the limit level.

Short Circuit Protection

The WD3102C has an advanced output short-circuit protection mechanism which prevents the IC from damage by unexpected applications. When the output becomes shorted to ground, and the output voltage is under the limit level with 1ms (typ.) duration, the bias function enters shutdown mode and can only re-start normal operation after triggering the SWIRE pin.

Over Temperature Protection

The WD3102C equips an over temperature protection circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down the bias operation when ambient temperature exceeds 140 °C. Once the ambient temperature cools down by approximately 15 °C, IC will automatically resume normal operation. To maintain continuous operation, the maximum junction temperature should be prevented from rising above 125 °C.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

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$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA} , is layout dependent. For WL-CSP-15B 1.39x2.07 (BSC) package, the thermal resistance, θ_{JA}, is 49.8°C/W on a standard JEDEC 51-7 four-layer thermal test board.

The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C－25°C) / (49.8°C /W) = 2W for WL-CSP-15B 1.39x2.07 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}.

PC Board Layout Considerations

For the best performance of WD3102C, the following PCB layout guidelines should be strictly followed.

1. For good regulation, place the power components as close to the IC as possible. The traces should be wide and short especially for the high current output loop.
2. The input and output bypass capacitor should be placed as close to the IC as possible and connected to the ground plane of the PCB.
3. The flying capacitor should be placed as close to the C1P/C1N/C2P/C2N pin as possible to avoid noise injection.
4. Minimize the size of the LXP node and keep the traces wide and short. Care should be taken to avoid running traces that carry any noise-sensitive signals near LXP or high-current traces.
5. Separate power ground (PGND) and analog ground (GND). Connect the GND and the PGND islands at a single end. Make sure that there are no other connections between these separate ground planes.

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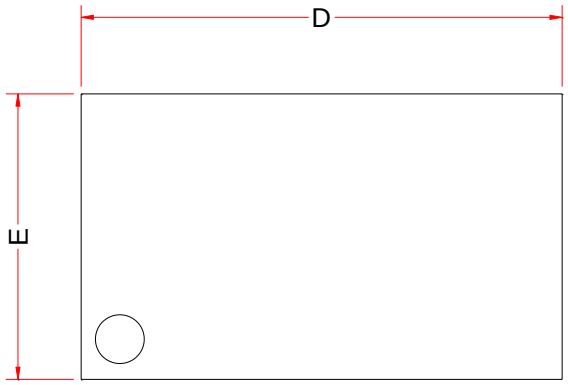
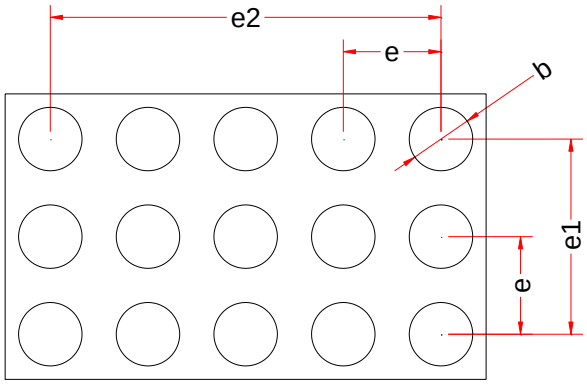
PACKAGE OUTLINE DIMENSIONS

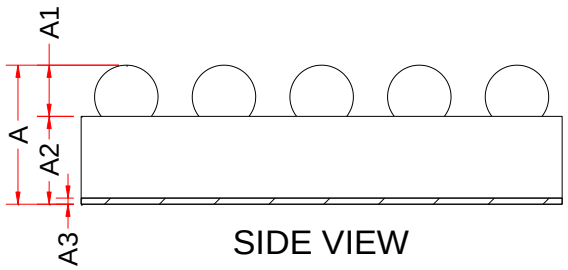
CSP-15L



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.51	0.56	0.61
A1	0.19	0.21	0.23
A2	0.32	0.35	0.38
A3	0.025REF		
b	0.24	0.26	0.28
D	1.94	1.97	2.00
E	1.14	1.17	1.20
e	0.40BSC		
e1	0.80BSC		
e2	1.60BSC		

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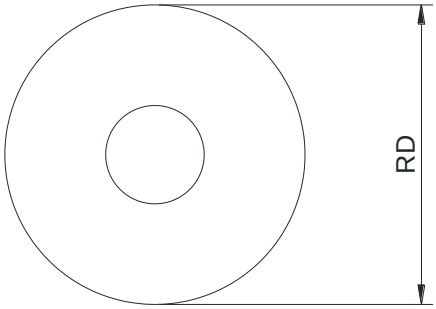
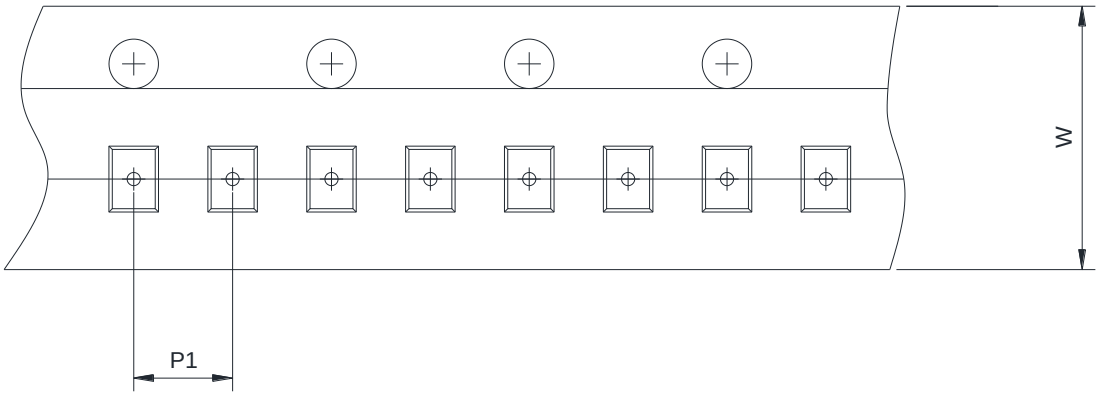
TAPE AND REEL INFORMATION

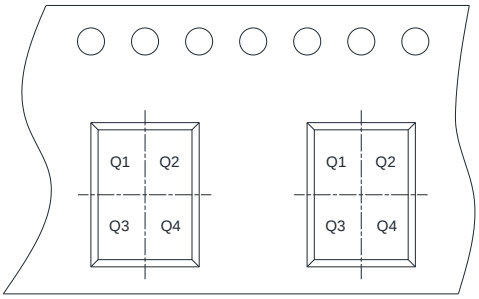
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



User Direction of Feed

RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm		
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4

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