WD1304E30

18V, 3A, High-Efficiency, Synchronous Step-Down Converter

Http//:www.ovt.com

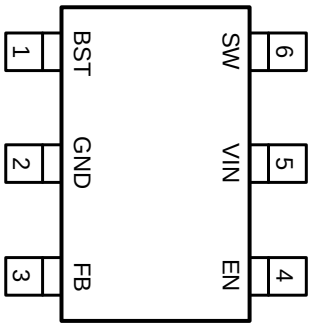
Descriptions

The WD1304E30 is a high efficiency, 760 kHz switch frequency, synchronous step-down DC-DC converter with delivering 3A current capability. The WD1304E30 operates over a wide input voltage range from 4.5V to 18V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

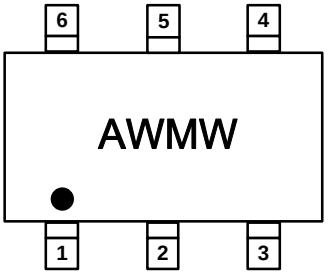
The WD1304E30 applies Constant-on-time (COT) control mode which provides very fast load transient response and easy loop design. The WD1304E30 integrates full protections features including short-circuit protection, over-current protection, under voltage protection and thermal shutdown to make the part operating safely.

The WD1304E30 is available in SOT-23-6L package. Standard product is Pb-free and Halogen-free.

SOT-23-6L



Pin configuration (Top view)



AW = Special code
M = Month code
W = Week code

Marking

Features

- Wide input voltage range of 4.5V to 18V
- Integrate 77mΩ (High Side) / 50mΩ (Low Side) Low $R_{DS(ON)}$ Power MOSFETs
- 340μA Low Quiescent Current
- High-efficiency synchronous-mode Operation
- Power save mode at light load
- Fast load transient response with COT control mode
- Over-current protection and Hiccup
- Output adjustable from 0.6V

Applications

- Set Top Box
- Access Point Router
- DSL Modem
- Flat-Panel Televisions and Monitors
- Security Cameras

Order information

Device	Package	Shipping
WD1304E30-6/TR	SOT-23-6L	3000/Reel&Tape

Typical Applications

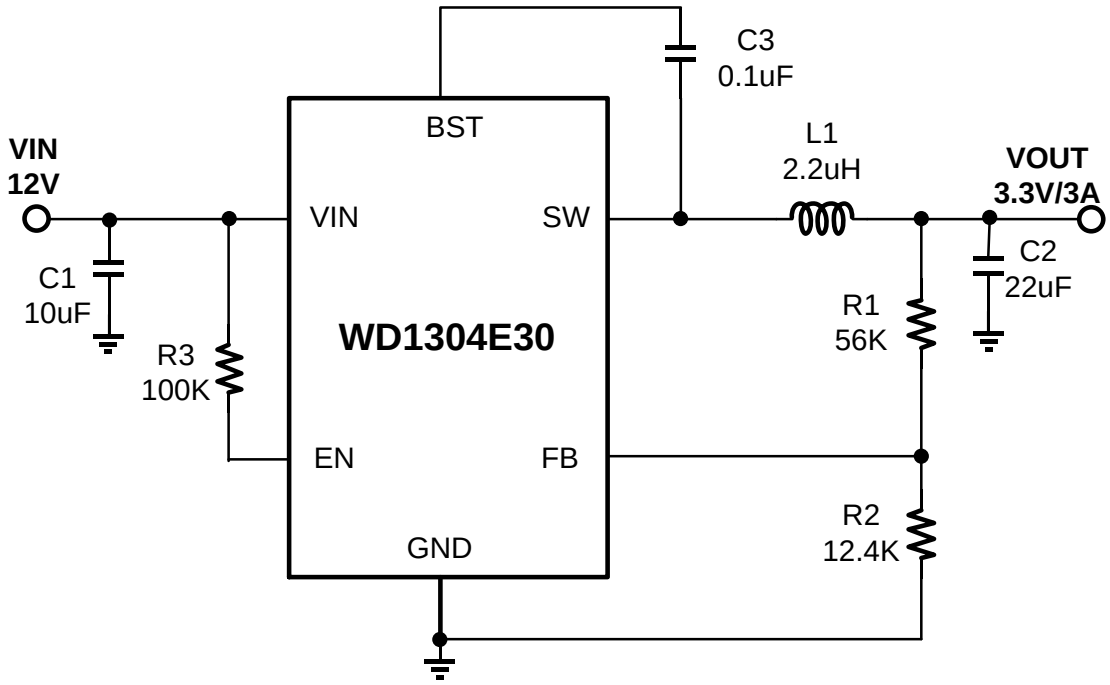
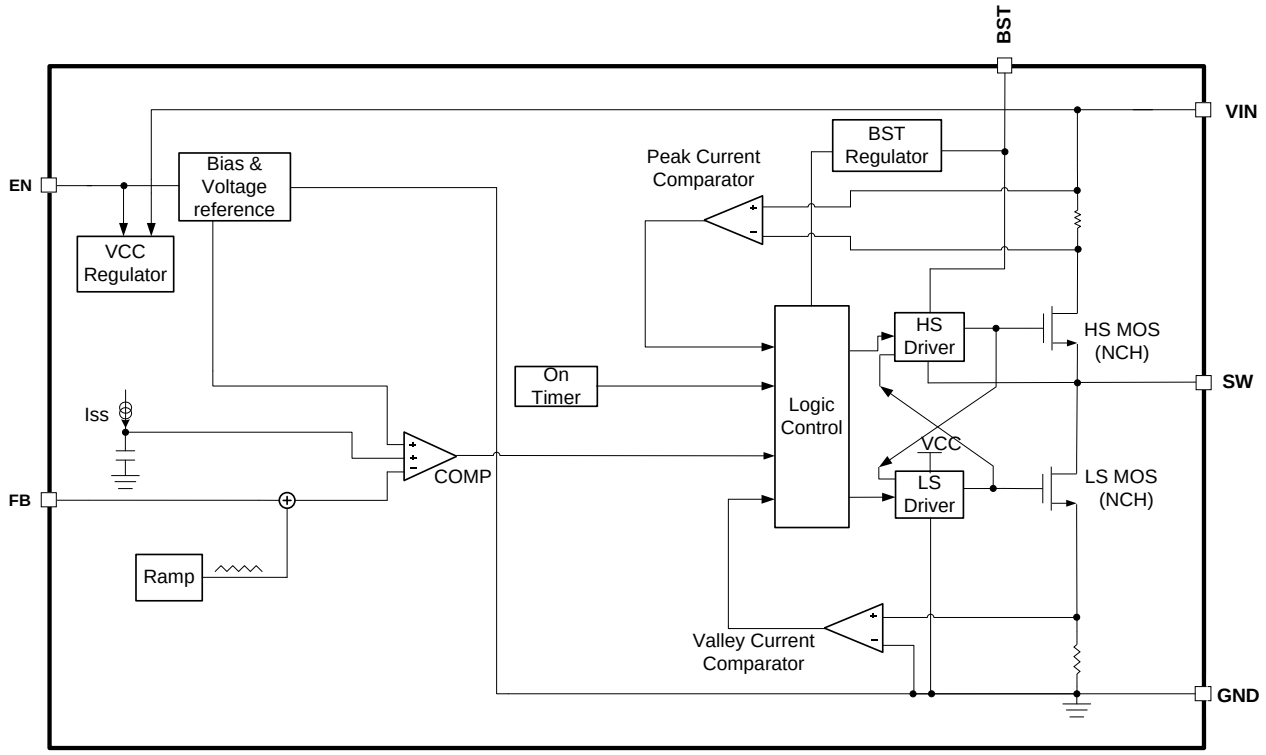


Fig1 Schematic Diagram

Pin Descriptions

No.	Symbol	Description
1	BST	Bootstrap pin. Connect a capacitor between SW and BST pins to form a floating supply across the high-side switch driver. Use a 0.1μF BST capacitor.
2	GND	System Ground pin. Reference ground of the regulated output voltage: requires extra care during PCB layout. Connect to GND with copper traces and vias.
3	FB	Converter feedback input. Connect to output voltage with feedback resistor divider.
4	EN	Enable input control pin. To active high for automatic start-up, EN can be connected to VIN directly or through a resistor.
5	VIN	Supply Voltage pin. Requires a cap to decouple the input rail. Connect using a wide PCB trace.
6	SW	Switch Output pin. Connect using a wide PCB trace.

Block Diagram



Absolute Maximum Ratings

Symbol	Characteristics	Rating	Unit
V_{IN}	Supply Voltage	-0.3 ~ 20	V
V_{SW}	Switch Output	-0.3 ~ 20	V
V_{BST}	Bootstrap Voltage	V_{SW} +5.5	V
V_{EN}	Enable Input Control	-0.3 ~ 20	V
V_{FB}	Feedback Voltage	-0.3~5.5	V
T_J	Junction Temperature	155	℃
θ_{JA}	JESD51-7	100	℃/W
θ_{JC}		55	
Lead Temperature		260	℃
Storage Temperature		-65 ~150	℃
Continuous Power Dissipation (T_A = +25°C) (2)		1.85	W

Note (1): Exceeding these ratings may damage the device.

Note (2): The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX) = (T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. θ_{JA} is tested based on EV5303-1.0 board.

Recommended Operation Conditions (3)

Symbol	Characteristics	Min	Typ	Max	Unit
V_{IN}	Supply Voltage	4.5	12	18	V
V_{OUT}	Output Voltage	V_{FB}		8	V
Operating Junction Temp. (T_J)	Operating temperature	-40	-	125	℃

Note (3): The device is not guaranteed to function outside of its operating conditions.

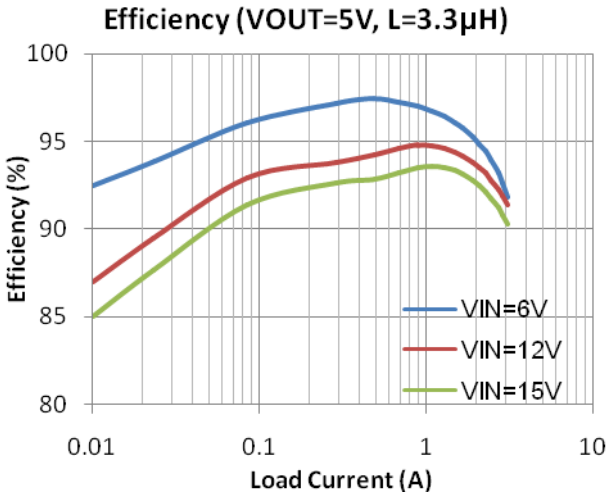
Electronics Characteristics (Ta=25°C, V_{IN}=12V, unless otherwise noted)

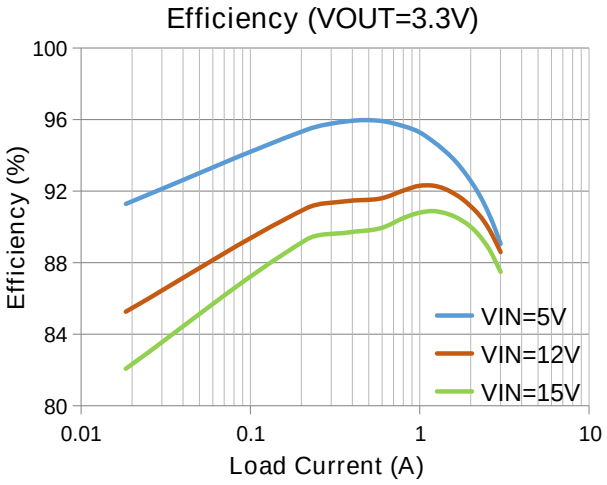
Description	Symbol	Test Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V			10	μA
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 1V, T_J=+25℃	244	340	436	uA
HS Switch-On Resistance	R_{on_HS}	V_{BST-SW}=5V		77		mΩ
LS Switch-On Resistance	R_{on_LS}			50		mΩ
Switch Leakage	SW_LKG	V_{EN} = 0V, V_{SW} =12V			1	μA
Valley Current Limit			3.1	3.7	4.6	A
ZCD		V_{IN}=12V, V_{OUT}=3.3V, L=2.2uH		80		mA
Oscillator Frequency	F_{SW}	V_{FB}=0.55V		760		kHz
Min_On_Time (4)	T_{ON_MIN}			65		ns
Min_Off_Time (4)	T_{OFF_MIN}			120		ns
Feedback Voltage	V_{REF}	T_J=+25℃	588	604	620	mV
Feedback Current	I_{FB}			18	60	nA
Hiccup threshold(H to L)	FB_{UV_th}	Hiccup entry (FB UV with deglitch 10us)		44%		V_{REF}
Hiccup duty cycle(4)	D_Hiccup			25		%
EN Rising Threshold	V_{EN_RISING}		1.1	1.2	1.4	V
EN Hysteresis	V_{EN_HYS}			165		mV
EN Input Current	I_{EN}	V_{EN}=2V		2.6	4	μA
		V_{EN}=0V		0		
VIN Under Voltage Lockout Threshold-Rising	$INUV_{TH}$		3.9	4.2	4.4	V
VIN Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			330		mV
Soft-Start Period	T_SS			1.1		ms
Thermal Shutdown(4)	T_SD			155		°C
Thermal Hysteresis(4)	TSD_HYS			20		°C

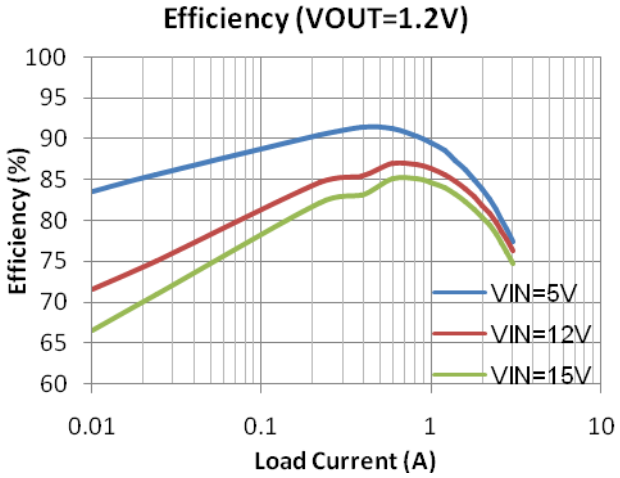
Note (4): Guaranteed by design and engineering sample characterization.

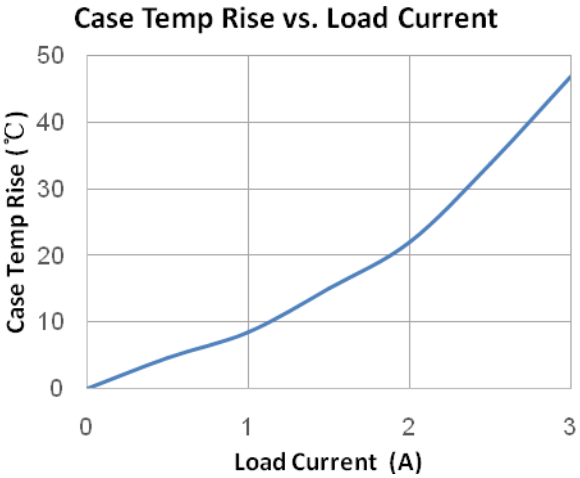
Typical Characteristics

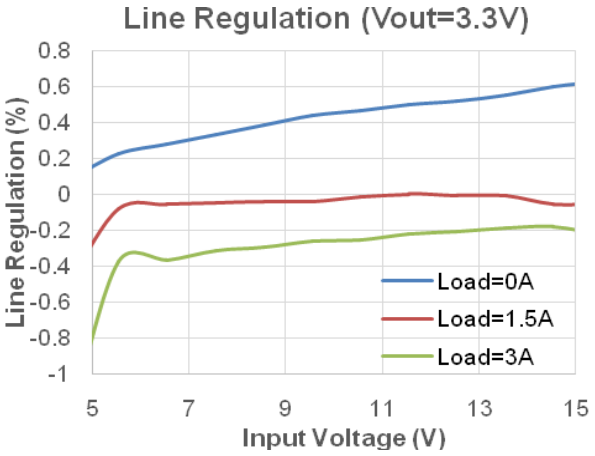
(V_{IN}=12V, V_{OUT}=3.3V, L=2.2μH, T_A=+25°C, unless otherwise noted)

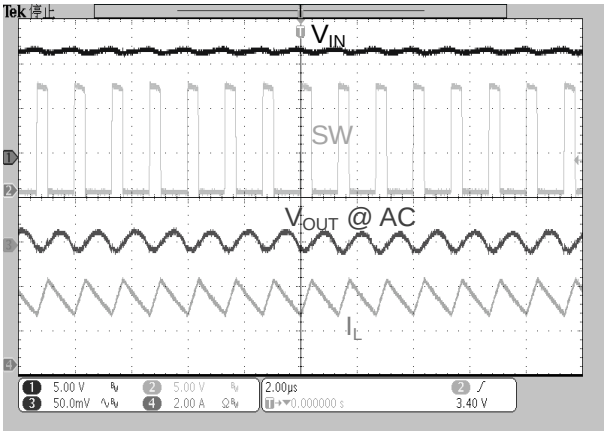




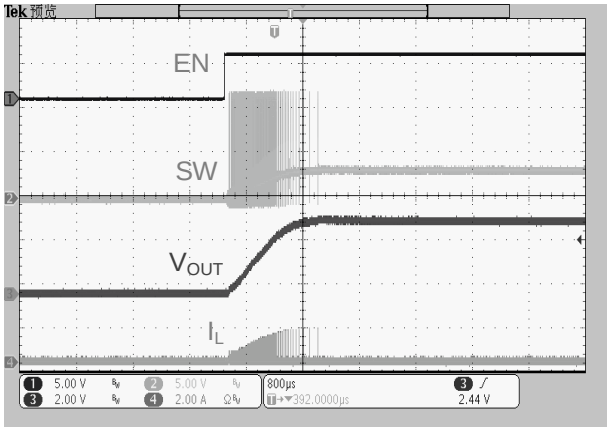




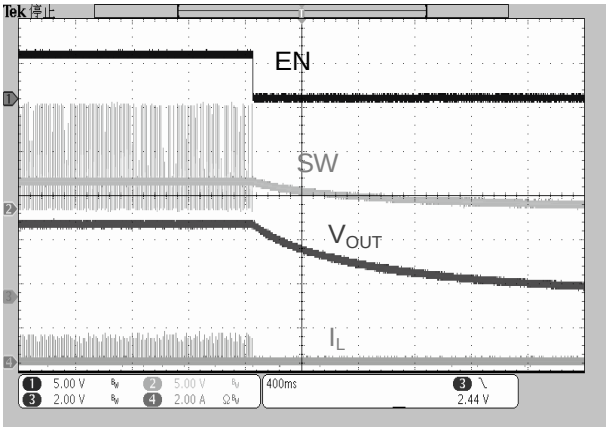




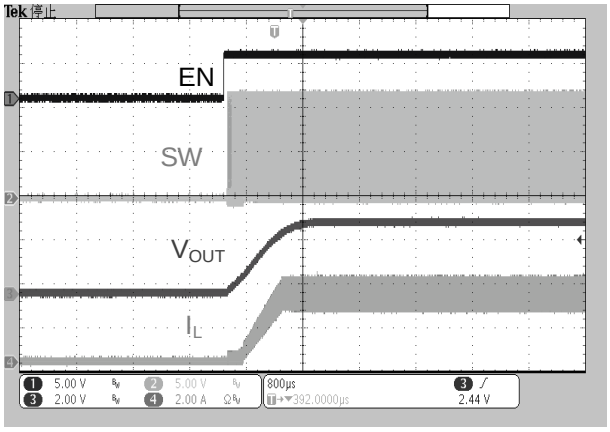
Output Ripple , I_{Load}=3A



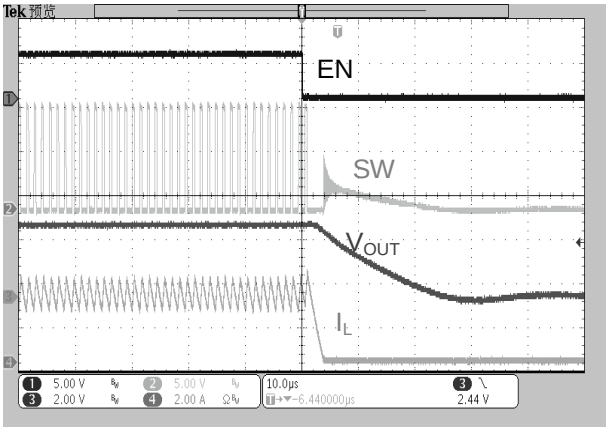
Start up through EN，I_{Load}=0A



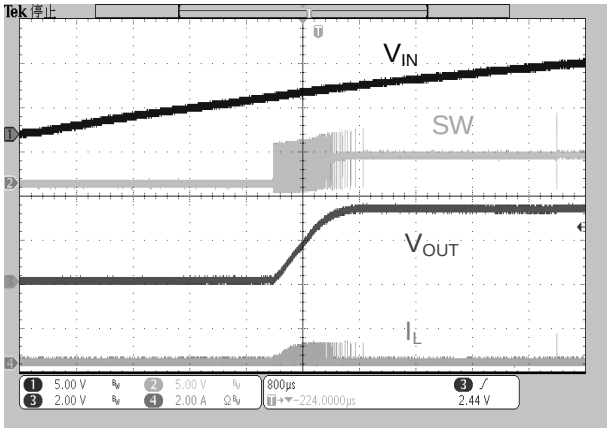
Shutdown through EN，I_{Load}=0A



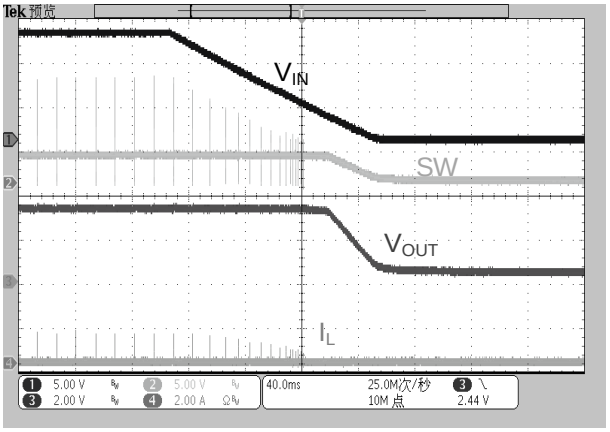
Start up through EN，I_{Load}=3A



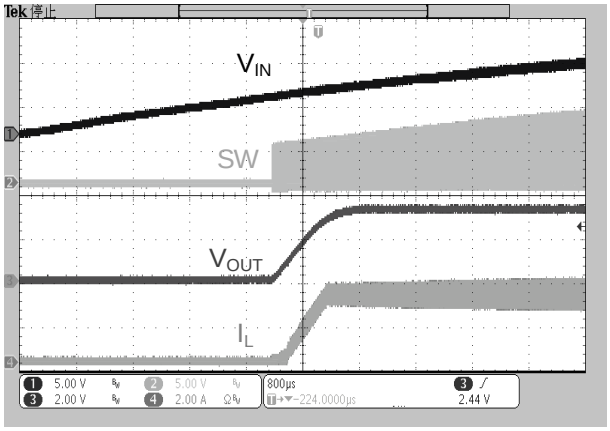
Shutdown through EN，I_{Load}=3A



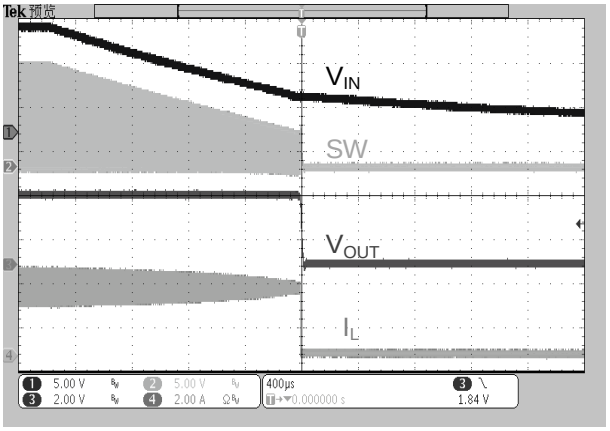
Start up through Input Voltage, I_{Load}=0A



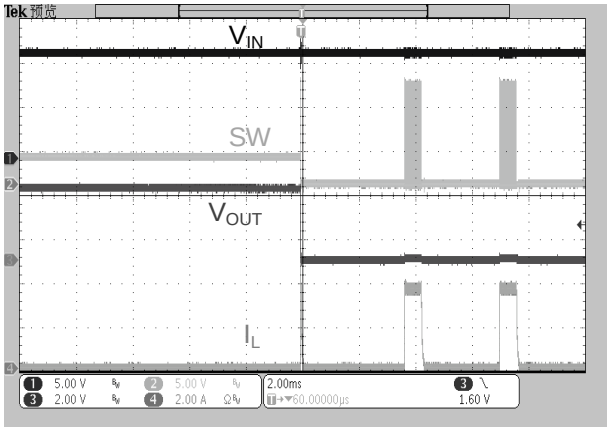
Shutdown through Input Voltage, I_{Load}=0A



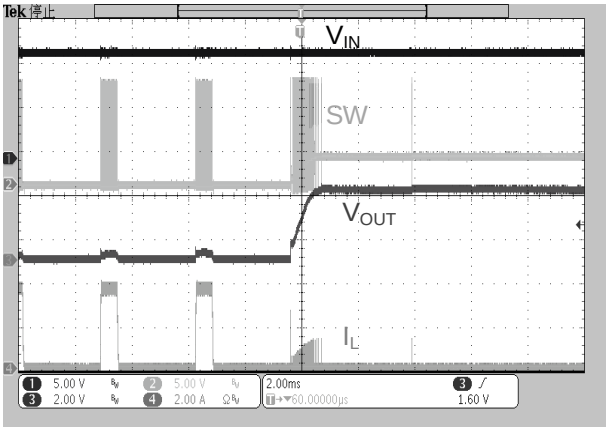
Start up through Input Voltage，I_{Load}=3A



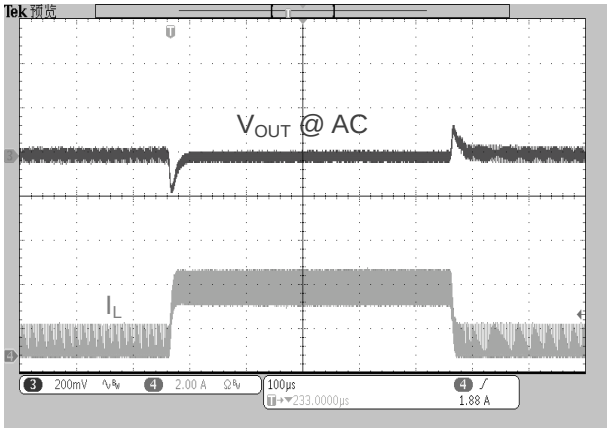
Shutdown through Input Voltage，I_{Load}=3A



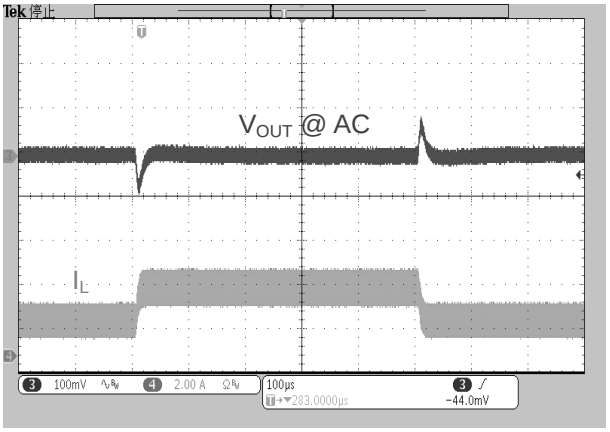
Output Short-circuit entry，I_{Load}=0A



Output Short-circuit Recovery，I_{Load}=0A



Transient Response，I_{Load}=0.3A to 3A, 2.5A/μs



Transient Response，I_{Load}=1.5A to 3A, 2.5A/μs

Operation Informations

The WD1304E30 is fully integrated, synchronous, rectified, step-down, switch-mode converter. Constant-on-time (COT) control is employed to provide fast transient response and ease loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned on when the FB voltage (V_{FB}) drops below the reference voltage (V_{REF}). The HS-FET is turned on for a fixed interval determined by the one-shot on-timer. The on-timer is determined by both the output voltage and input voltage to make the switching frequency fairly constant over the input voltage range. After the on period elapses, the HS-FET is turned off until the next period begins. By repeating this operation, the converter regulates the output voltage.

Continuous conduction mode (CCM) occurs when the output current is high and the inductor current is always above zero amps. The low side MOSFET is turned on when the high side MOSFET is in its off state to minimize conduction loss. There is a dead short between the input and GND if both the HS-FET and LS-FET are turned on at the same time. This is called a shoot-through. To prevent a shoot-through, a dead time is generated internally between the HS-MOSFET off and LS-MOSFET on, or LS-MOSFET off and HS-MOSFET on.

When the WD1304E30 works in PFM mode during light-load operation, the WD1304E30 reduces the switching frequency automatically to maintain high efficiency, and the inductor current drops almost to zero. When the inductor current reaches zero, the low-side driver enters tri-state (high-Z). The output capacitors discharge slowly to GND through FB divider resistors. When VFB drops below the reference voltage, the HS-FET is turned on. This operation improves device efficiency greatly when the output current is low.

Light-load operation is also called skip mode because the HS-FET does not turn on as frequently as it does in heavy-load conditions. The frequency at which the HS-FET turns on is a function of the output current. As the output current increases, the time period that the current modulator regulates becomes shorter, and the HS-FET turns on more frequently. The switching frequency increases in turn. The output current reaches critical levels when the current modulator time is zero, and can be determined with Equation (1):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (1)$$

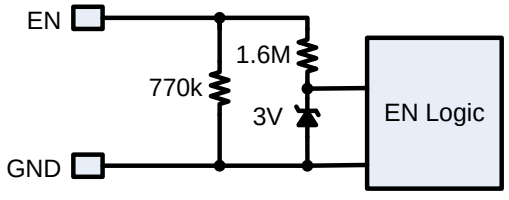
The WD1304E30 reverts to PWM mode once the output current exceeds the critical level. Afterward, the switching frequency remains fairly constant over the output current range.

Under Voltage Lockout (UVLO)

Under-voltage lock out protection (UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut down. This protection is non-latching. The UVLO rising threshold is about 4.2V, while its falling threshold is 3.87V.

Enable (EN) Control

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 770 kΩ resistor from EN to GND allows EN to be floated to shut down the chip. EN is clamped internally using a 3V series Zener diode (see Figure below). EN can connected to VIN directly to save one pull up resistor.



Zener Diode between EN and GND

Over-Current Protection (OCP) and Short Circuit Protection (SCP)

The WD1304E30 has valley current-limit control. During LS-FET on, the inductor current is monitored. When the sensed inductor current reaches the valley current limit, the LS-MOSFET limit comparator turns over. The device enters over current protection (OCP) mode and the HS-FET waits until the valley current limit disappears before turning on again. The output voltage drops until V_{FB} is below the under voltage (UV) threshold (typically 44% below the reference). Once UV is triggered, the WD1304E30 enters hiccup mode to restart the part periodically. During OCP, the device attempts to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft start, and attempts to soft start again automatically. If the over-current condition still holds after the soft start ends, the device repeats this operation cycle until the over-current condition is removed and the output rises back to regulation levels. OCP is a non-latch protection.

Soft Start and Pre-Biased Soft Start

Soft start (SS) prevents the converter output voltage from overshooting during start-up. The WD1304E30 has an internal 1.1ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator. If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This is a non-latch protection.

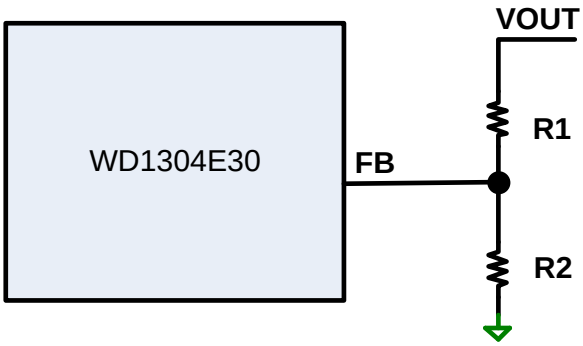
Application Informations

Setting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation (2) to calculate V_{OUT}. To improve efficiency at light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the FB input current will be more noticeable.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

The feedback circuit is shown in below:



Setting the Inductor

An inductor is necessary to supply a constant current to the output load while being driven by the switched input voltage. A larger inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be between 30% to 40% of the maximum output current, and ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Selecting the Input Capacitor

The device requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (6):

$$I_{CIN} = \frac{1}{2} \times I_{OUT} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (8)$$

A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor from VIN pin to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (9)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (10)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (11)$$

The table below listed the recommended parameters for common output voltages:

VOUT	Inductor	Output Capacitor	R1	R2
5V	3.3uH(5)	22uF	56kΩ	7.6kΩ
3.3V	2.2uH(5)	22uF	56kΩ	12.4kΩ
1.2V	2.2uH(5)	22uF	56kΩ	56kΩ

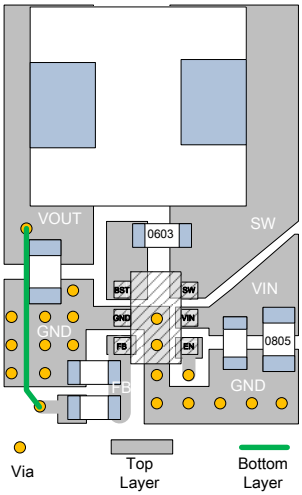
Note (5): Strongly recommended no less than this value

PC Board Layout Considerations

A good circuit board layout aids in extracting the most performance from the WD1304E30. Poor circuit layout degrades the output ripple and the electromagnetic interference (EMI) or electromagnetic compatibility (EMC) performance.

The evaluation board layout is optimized for the WD1304E30. Use this layout for best performance. If this layout needs changing, use the following guidelines:

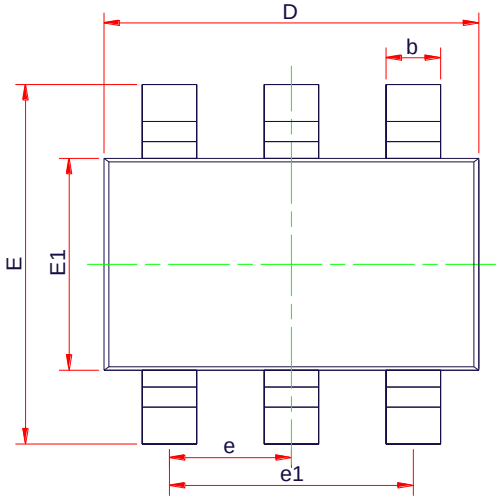
- V_{IN} and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- The distance between input capacitor and the device should be no larger than 1mm to minimize V_{IN} voltage spike.
- Do not allow switching current to flow under the device.
- A separate V_{OUT} path should be connected to the upper feedback resistor.
- Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
- The trace of the FB node should be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.



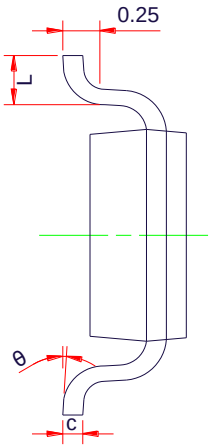
Recommended PCB layout

PACKAGE OUTLINE DIMENSIONS

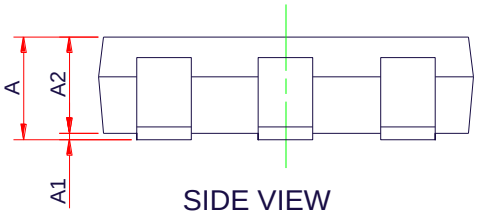
SOT-23-6L



TOP VIEW



SIDE VIEW

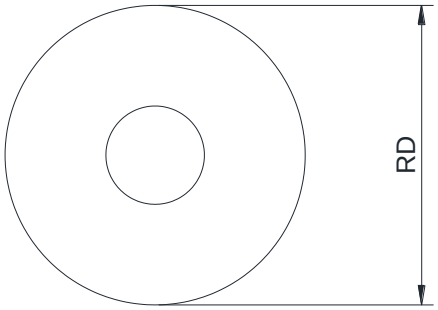


SIDE VIEW

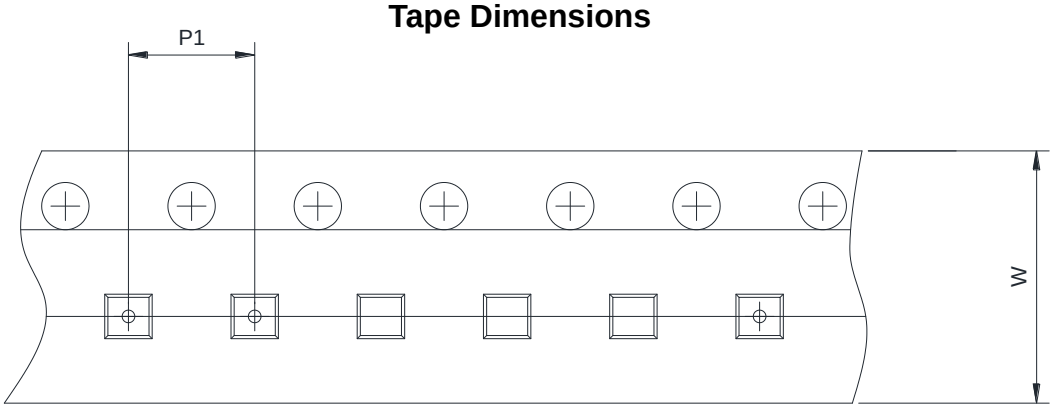
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	-	-	1.25
A1	0.04	-	0.10
A2	1.00	1.10	1.20
b	0.33	-	0.41
c	0.15	-	0.19
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
θ	0°	-	8°

TAPE AND REEL INFORMATION

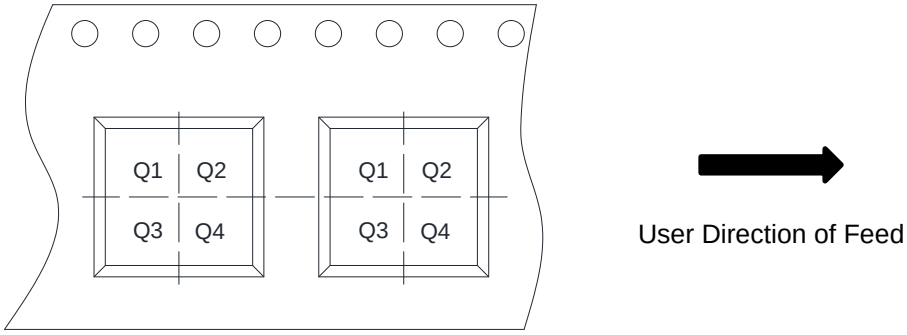
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch ☐ 13inch
W	Overall width of the carrier tape	☑ 8mm ☐ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☑ 4mm ☐ 8mm
Pin1	Pin1 Quadrant	☐ Q1 ☐ Q2 ☑ Q3 ☐ Q4