WD10721

2A Buck Converter with Light load Mode

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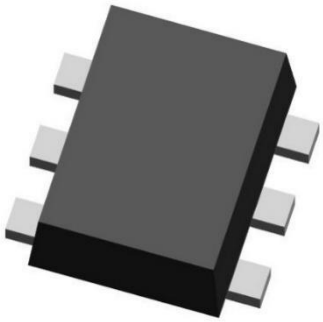
Descriptions

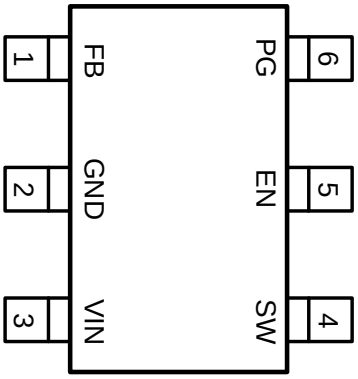
WD10721 is a synchronous Buck DC-DC converters optimized for high efficiency and compact solution size. The device integrates switches capable of delivering an output current up to 2 A. At PWM mode, the device operates in quasi fixed frequency constant on time mode with 2.1MHz switching frequency. In shutdown, the current consumption is reduced to less than 2 μA.

An internal soft start circuit limits the inrush current during startup. Other features like over current protection, and thermal shutdown protection are built-in.

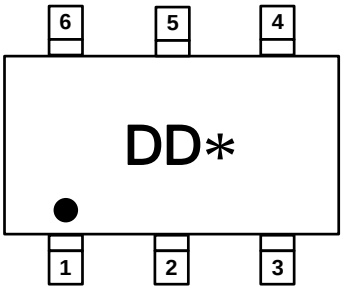
The WD10721 is available in SOT-563 package. Standard product is Pb-free and Halogen-free.



SOT-563



Pin configuration (Top view)



DD = Device name

*** = Month code**

Marking

Features

- Input Voltage Range of 2.5V to 5.5V
- Power saving mode at light load
- Up to 95% Efficiency
- Integrate 125mΩ (High Side) / 65mΩ (Low Side) Low $R_{DS(ON)}$ Power MOSFETs
- Adjustable Output Voltage from 0.6 V to VIN
- 100% Duty Cycle for Lowest Dropout
- 2.1 MHz Typical Switching Frequency
- 240 μS Fast Turn on Time
- 4 mS Fast Output Discharge Time
- Hiccup mode Over-current Protection
- Thermal Shutdown Protection

Applications

- General Purpose POL Supply
- Set Top Box
- Network Video Camera
- Wireless Router
- Solid State Driver / Hard Disk Driver
- Smartphone

Order information

Device	Package	Shipping
WD10721V-6/TR	SOT-563	3000/Reel&Tape

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Typical Applications

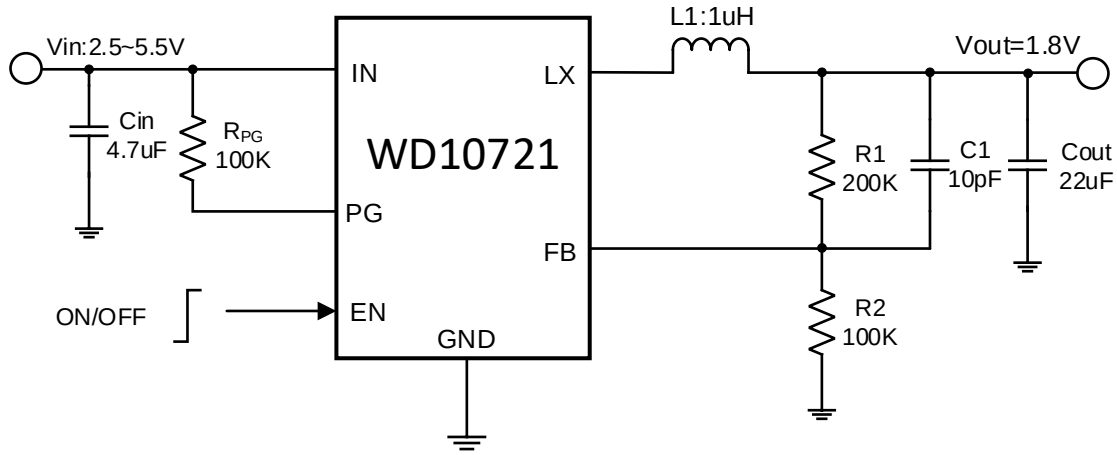
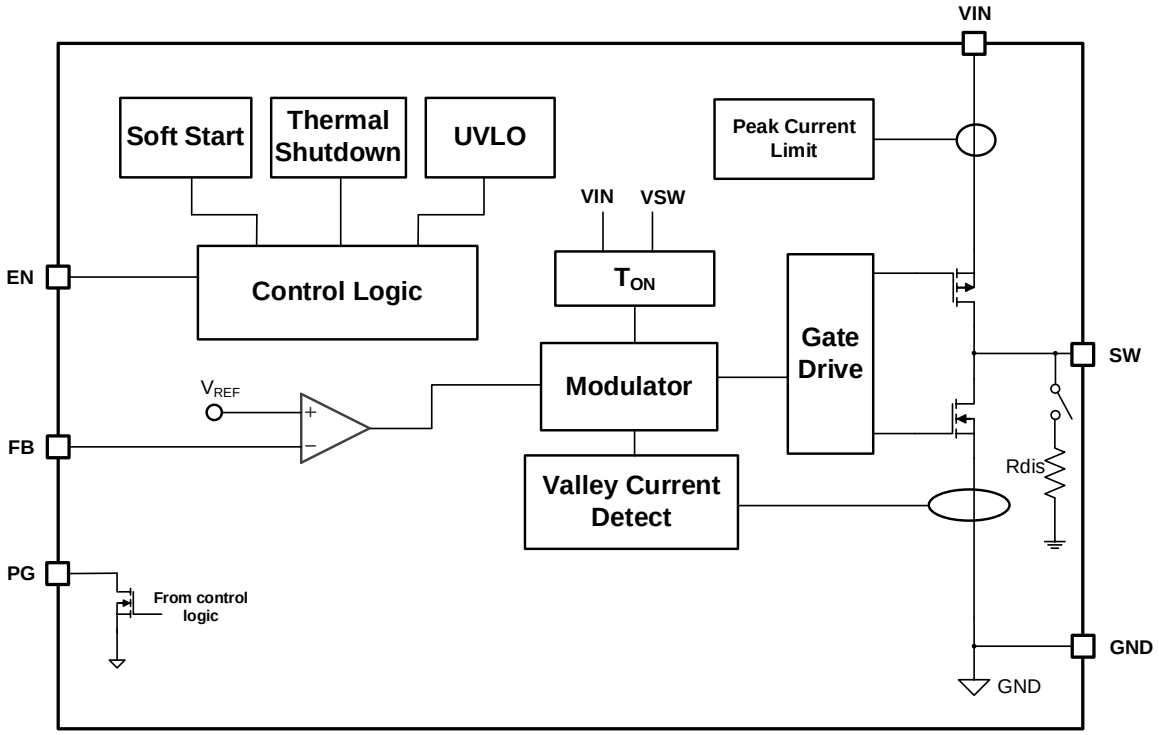


Fig1 Schematic Diagram

Pin Descriptions

No.	Symbol	Description
1	FB	Converter feedback input. Connect to output voltage with feedback resistor divider.
2	GND	System Ground pin. Reference ground of the regulated output voltage: requires extra care during PCB layout. Connect to GND with copper traces and vias.
3	VIN	Supply Voltage pin. Requires a cap to decouple the input rail. Connect using a wide PCB trace.
4	SW	Switch pin connected to the internal FET switches and inductor terminal. Connect the inductor of the output filter using a wide PCB trace to this pin.
5	EN	Device enable logic input. Logic high enables the device, logic low disables the device and turns it into shutdown. Do not leave floating. To active high for automatic start-up, EN can be connected to VIN directly or through a resistor.
6	PG	Power Good indication. Open Drain Output.

Block Diagram



Absolute Maximum Ratings(1)

Symbol	Characteristics	Rating	Unit
V_{IN} ,V_{EN}, V_{PG}	-	-0.3 ~ 6	V
V_{SW}(DC)	Switch Output	-0.3 ~ V_{IN}+0.3	V
V_{SW} (AC, less than 10ns)	Switch Output	-3.0 ~ 9	V
V_{FB}	Output Voltage Feedback	-0.3 ~ 3	V
T_J	Operation Junction Temperature	-40 ~ 150	℃
θ_{JA}	-	142	℃/W
θ_{JC}		51	
T_{stg}	Storage Temperature	-65 ~150	℃
HBM	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
CDM	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

Note (1): Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operation Conditions

Symbol	Characteristics	Min	Typ	Max	Unit
V_{IN}	Supply Voltage	2.5		5.5	V
V_{OUT}	Output Voltage	V_{FB}		V_{IN}	V
I_{OUT}	Output Current	0		2	A
T_J	Operating Junction Temp.	-40		125	℃

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Electronics Characteristics (Ta=25°C, V_{IN}=5V, unless otherwise noted)(2)

Description	Symbol	Test Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{SD}	V_{EN} = 0V		0.01	2	μA
Supply Current (Quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.63V		40		μA
HS Switch-On Resistance	R_{on_HS}	I_{SW}=100mA , V_{IN}=3.6V		125		mΩ
LS Switch-On Resistance	R_{on_LS}	I_{SW}= -100mA , V_{IN}=3.6V		65		mΩ
Current Limit	I_{LIM}	High-side FET current limit	3			A
Switching Frequency	F_{SW}			2100		kHz
Max Duty Cycle	D_{MAX}		100			%
Feedback Voltage	V_{REF}	T_J= 25℃	594	600	606	mV
		T_J= -40℃ to 125℃	588		612	
Feedback Current	I_{FB}	V_{FB}=0.63V		50	100	nA
EN Rising Threshold	V_{EN_RISING}		1.2			V
EN Falling Threshold	$V_{EN\_FALLING}$				0.4	V
EN Input Current	I_{EN}	V_{EN}=2V		0.4		μA
		V_{EN}=0V		0		
VIN Under Voltage Lockout Threshold	$INUV_{TH}$	Rising		2.3	2.45	V
VIN Under Voltage Lockout Threshold Hysteresis	$INUV_{HYS}$			100		mV
Soft-Start Period	T_SS	From EN High to Vout*90%		120	240	μS
Discharge Resistance	Rdis			45		Ohm
Fast Discharge Time	Tdis	Cout=30μF, output discharge to below 100mV		4		mS
PG_Pull down resistance	Rpg			275	400	Ohm
Power Good Threshold	V_{PG}	V_{FB} rising, referenced to V_{FB} nominal		90		%
		V_{FB} falling, referenced to V_{FB} nominal		83		%
Power Good Delay Time	T_{PG_DLY}	From Vout *90% to Power Good ON		30		μS
Thermal Shutdown	T_SD			160		°C
Thermal Hysteresis	TSD_HYS			25		°C

Note (2): Guaranteed by design and engineering sample characterization.

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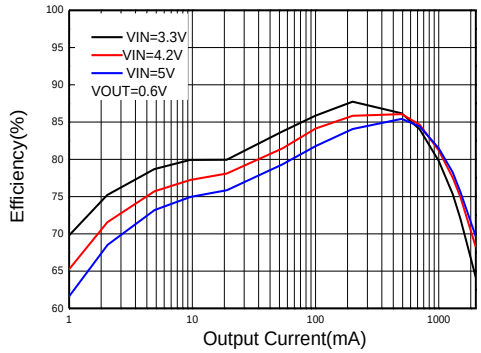
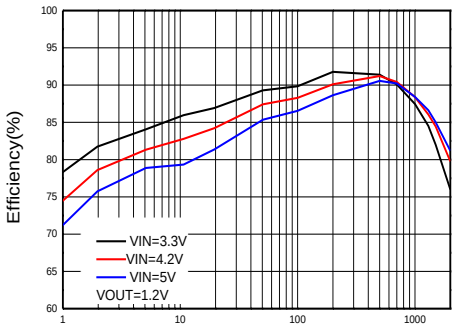
Typical Characteristics

(V_{IN}=5V, V_{OUT}=1.8V, L=1.0µH, C_{IN}=4.7uF, C_{OUT}=22uF, T_A=+25°C, unless otherwise noted)



Efficiency vs Output Current



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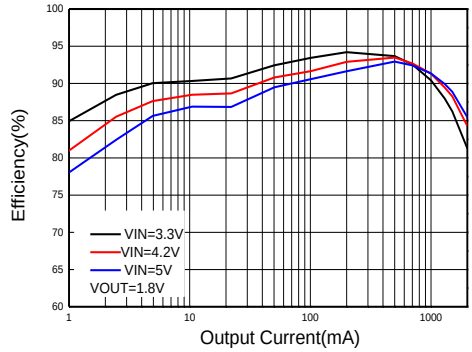
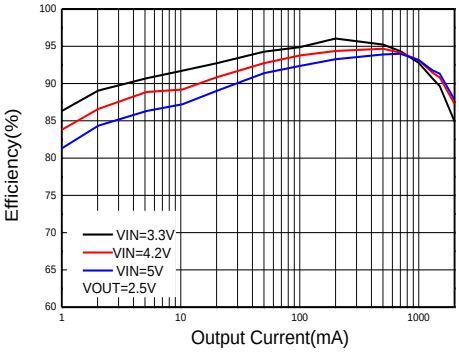
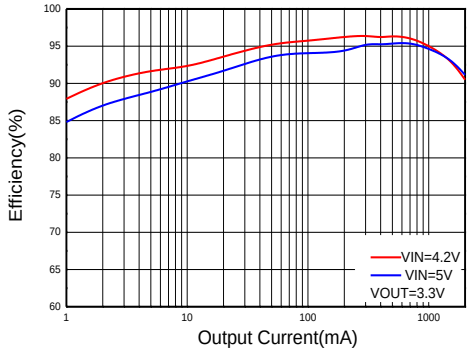


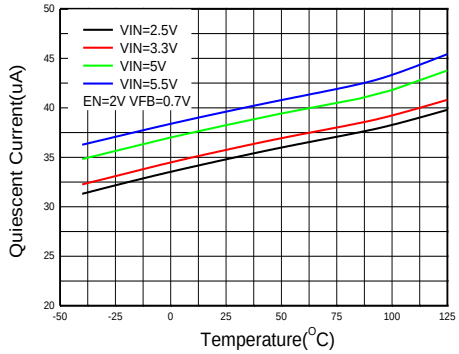
Efficiency vs Output Current



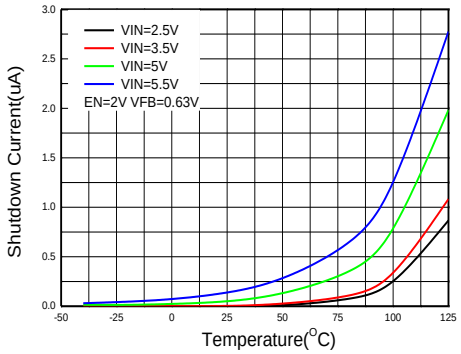
Efficiency vs Output Current



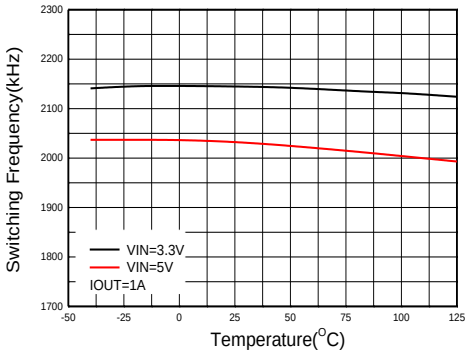
Efficiency vs Output Current



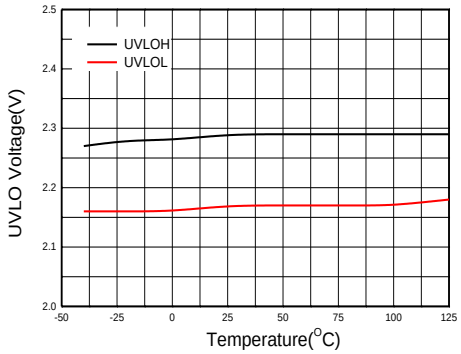
Quiescent current vs Temperature



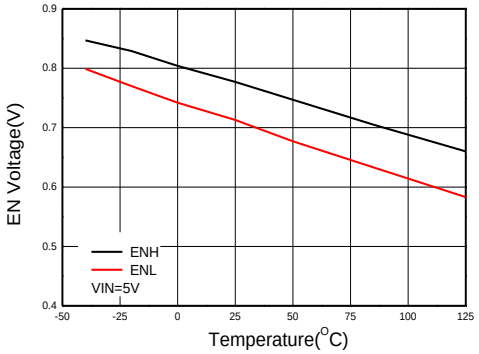
Shutdown current vs Temperature



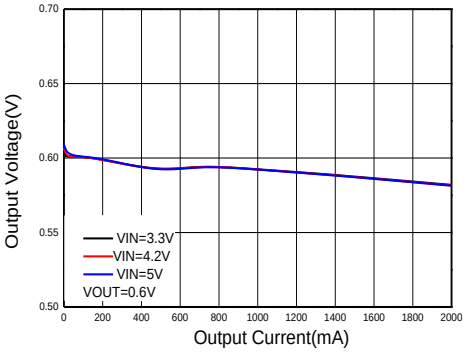
Switching frequency vs Temperature



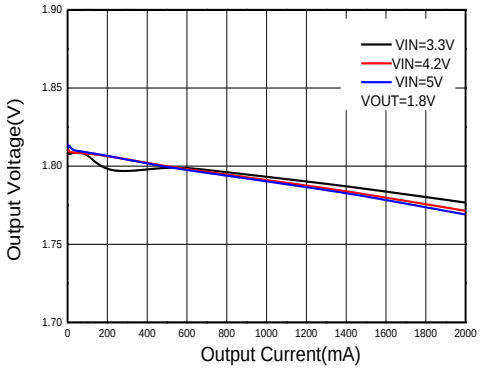
UVLO vs Temperature



Enable Threshold vs Temperature



Output Voltage vs Output Current



Output Voltage vs Output Current

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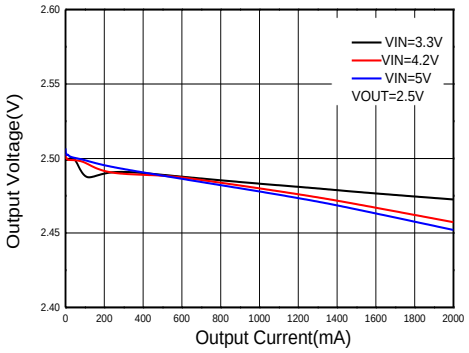
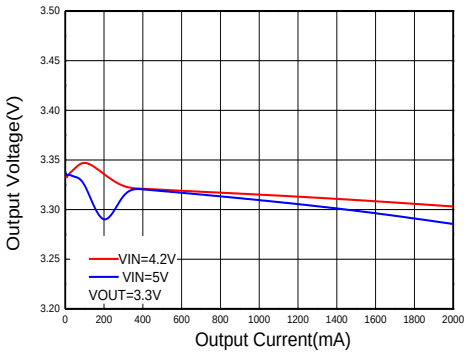
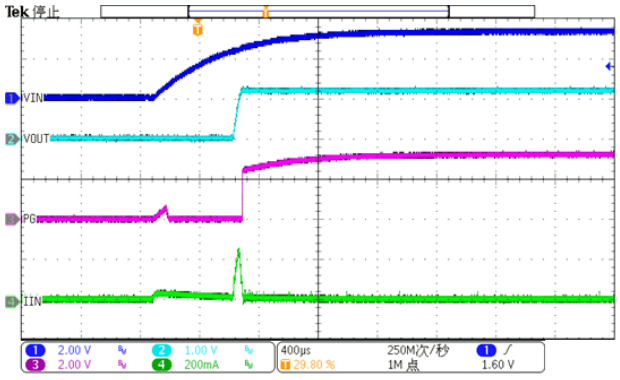


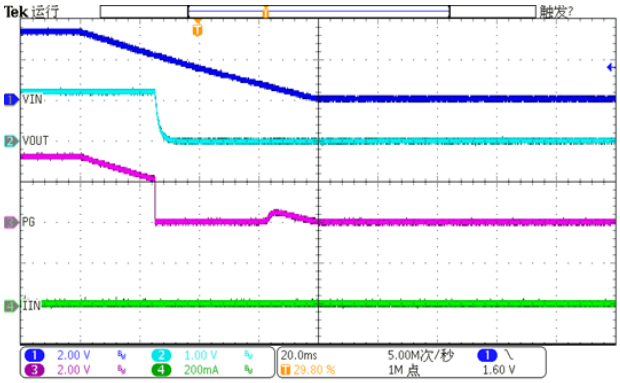
Output Voltage vs Output Current



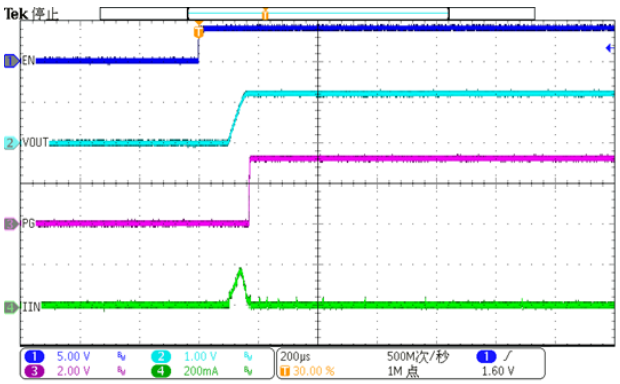
Output Voltage vs Output Current



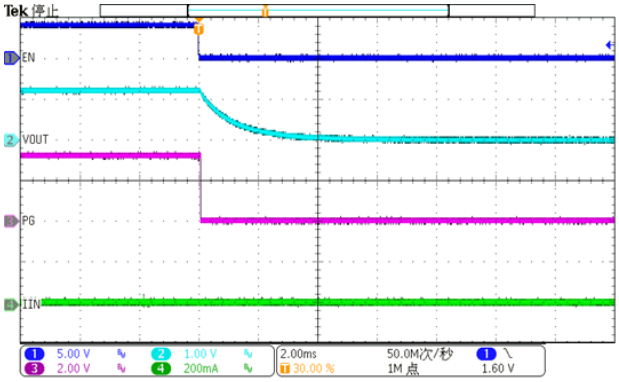
Start up from V_{IN}, V_{IN}= 3.3V,V_{OUT}=1.2V,I_{OUT}=0A



Shut down from V_{IN}, V_{IN}= 3.3V,V_{OUT}=1.2V,I_{OUT}=0A



Start up from EN, V_{IN}= 3.3V,V_{OUT}=1.2V,I_{OUT}=0A



Shut down from EN, V_{IN}= 3.3V,V_{OUT}=1.2V,I_{OUT}=0A

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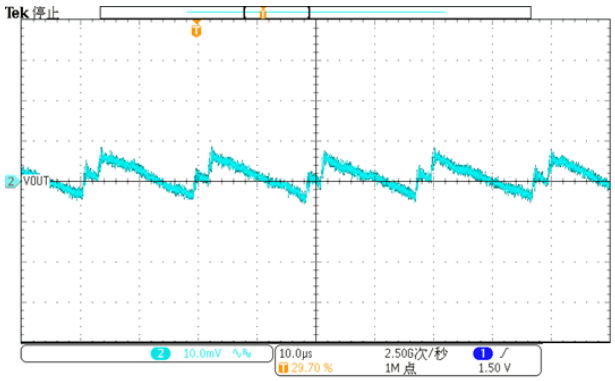
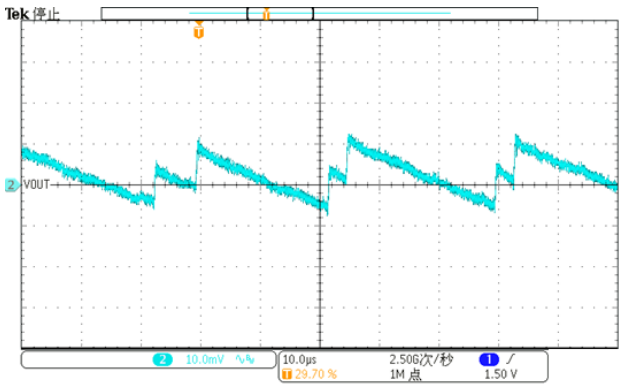
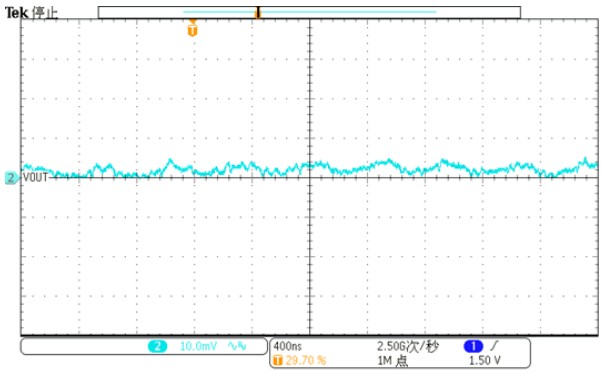


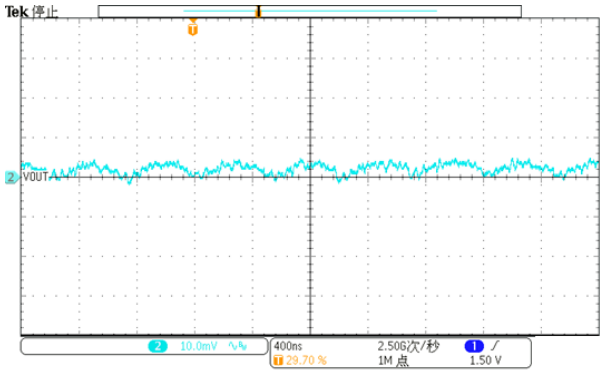
V_{IN}= 3.3V,V_{OUT}=1.8V; I_{OUT}=10mA



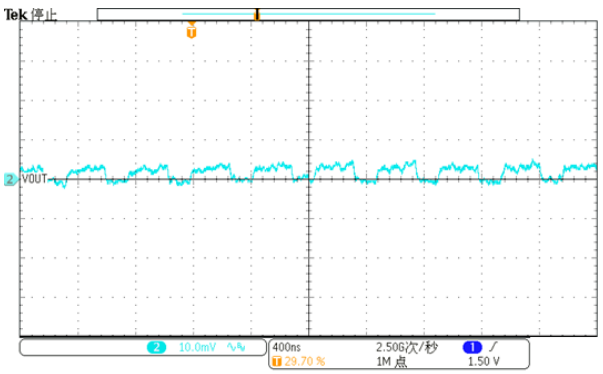
V_{IN}= 5V,V_{OUT}=1.8V; I_{OUT}=10mA



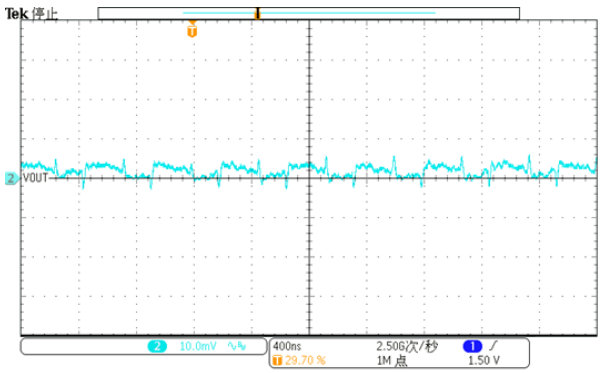
V_{IN}= 3.3V,V_{OUT}=1.8V; I_{OUT}=0.5A



V_{IN}= 5V,V_{OUT}=1.8V; I_{OUT}=0.5A



V_{IN}= 3.3V,V_{OUT}=1.8V; I_{OUT}=2A



V_{IN}= 5V,V_{OUT}=1.8V; I_{OUT}=2A

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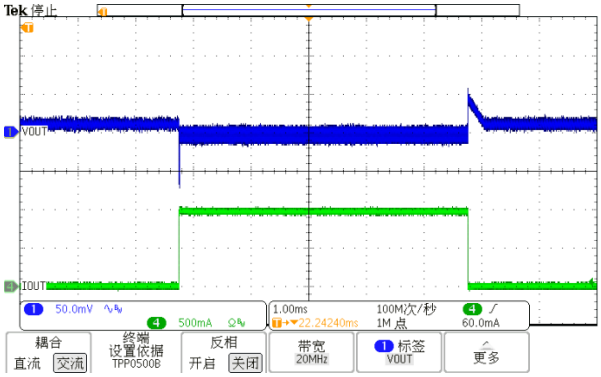
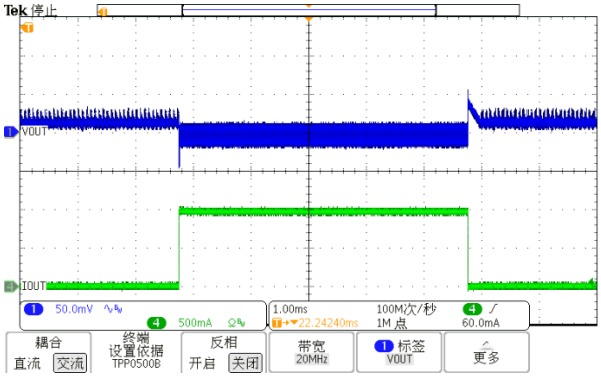
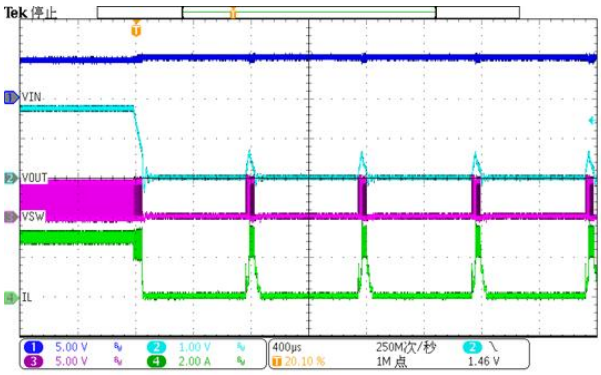


Load Transient, V_{IN}= 3.3V,V_{OUT}=1.8V; I_{OUT}=1mA~1A



Load Transient, V_{IN}= 5V,V_{OUT}=1.8V; I_{OUT}=1mA~1A



V_{IN}= 5.0V, V_{OUT}=1.8V, I_{OUT}=Short to GND

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Operation Informations

The WD10721 is a high-efficiency synchronous step-down converter. The device operates with an adaptive on time valley current control scheme. The device operates at typically 2.1MHz frequency Constant On time mode. Basing on the V_{IN}/V_{OUT} ratio, internal circuit sets required on time for high side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current. At light load the device operates in PFM mode to realize high efficiency

Enabling/Disabling the Device

The WD10721 is enabled by setting the EN input to a logic High. Accordingly, a logic Low disables the device. If the device is enabled, the internal power stage starts switching and regulates the output voltage to the set point voltage. The EN input must be terminated and should not be left floating.

100% Duty Cycle Low Dropout Operation

The WD10721 offers 100% duty cycle operation mode. In this mode, the high-side MOSFET switch is constantly turned on and the low-side MOSFET is switched off. The minimum input voltage to maintain output regulation, depending on the load current and output voltage, is calculated as:

$$V_{IN(MIN)} = V_{OUT} + I_{OUT} \times (R_{DS(ON)} + R_L)$$

where

- $R_{DS(ON)}$ = High side FET on-resistance
- R_L = Inductor ohmic resistance (DCR)

Soft Startup

After enabling WD10721, internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage in 120µS typically. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device is able to start into a pre-biased output capacitor. The converter starts with the applied bias voltage and ramps the output voltage to its nominal value.

Switch Current Limit

The switch current limit prevents the WD10721 from high inductor current and drawing excessive current from a battery or input voltage rail. Excessive current might occur with a heavy load or shorted output circuit condition. The device adopts the peak current limit control by sensing the current of the high-side switch. Once the high-side switch current limit is reached, the high-side switch is turned off and low-side switch is turned on to ramp down the inductor current with an adaptive off-time.

Under Voltage Lockout (UVLO)

To avoid mis-operation of the WD10721 at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO} with V_{HYS_UVLO} hysteresis.

Output Fast discharge

The device has built in discharge circuit. When disabled or in UVLO, the output capacitor will be discharged through the internal discharge resistor which is typically 45 Ohm.

Thermal Shutdown

The WD10721 enters thermal shutdown once the junction temperature exceeds the thermal shutdown rising threshold, T_{JSD}. Once the junction temperature falls below the falling threshold, the device returns to normal operation automatically.

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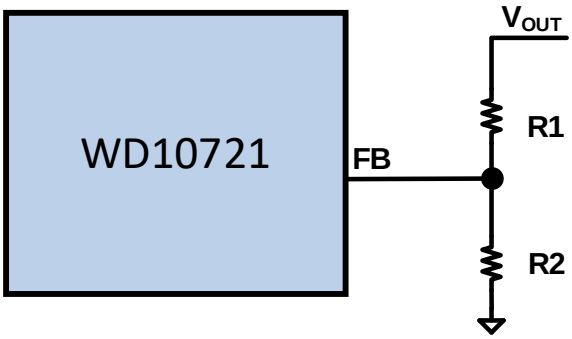
Application Informations

Setting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation (1) to calculate V_{OUT}. To improve efficiency at light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the FB input current will be more noticeable.

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

The feedback circuit is shown in below:



Setting the Inductor

An inductor is necessary to supply a constant current to the output load while being driven by the switched input voltage. A larger inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical footprint, higher series resistance, and lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be between 30% and 40% of the maximum output current, and ensure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated with Equation (2):

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Where ΔI_L is the peak-to-peak inductor ripple current. The inductor should not saturate under the maximum inductor peak current. The peak inductor current can be calculated with equation (3):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (3)$$

Selecting the Input Capacitor

The device requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use ceramic capacitors placed as close to VIN as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated with Equation (4):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (5):

$$I_{CIN} = \frac{1}{2} \times I_{OUT} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (7):

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$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (7)$$

A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor from VIN pin to ground is optional to provide additional high frequency filtering.

Selecting the Output Capacitor

An output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (8)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (10):

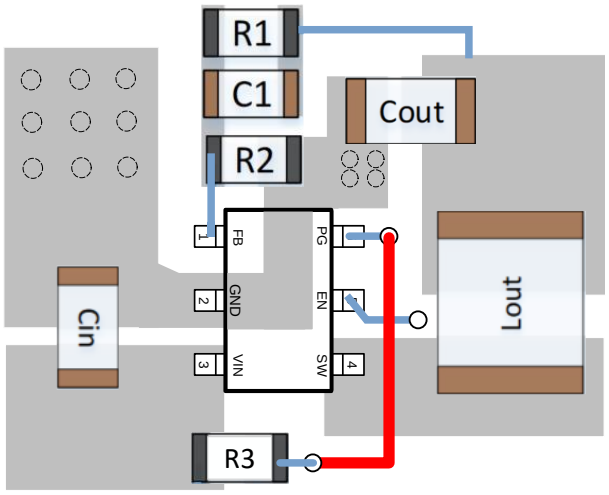
$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (10)$$

PC Board Layout Considerations

A good circuit board layout aids in extracting the most performance from the WD10721. Poor circuit layout degrades the output ripple and EMI or EMC performance.

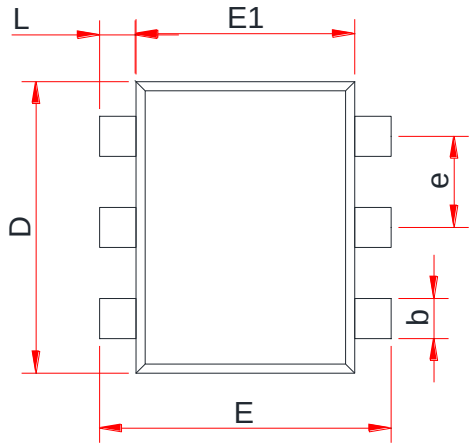
The evaluation board layout is optimized for the WD10721. Use this layout for best performance. If this layout needs changing, use the following guidelines:

- Use wide and short traces for power paths (such as VIN, SW and GND) to improve efficiency and reduce parasitic inductance.
- The input low-ESR ceramic capacitor should be connected to the VIN and GND pin as close as possible to the IC.
- Arrange a “quiet” path for output voltage sense and feedback network, and make it surrounded by a ground plane once possible. Place feedback network close to IC.
- GND trace that connect Cin, GND pin, Cout should be as short and wide as possible to minimize the trace impedance, big GND plane or layer is strongly recommended to improve thermal and noise performance.

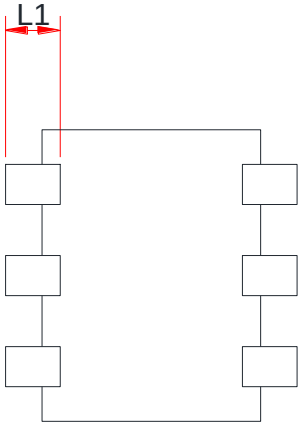


PACKAGE OUTLINE DIMENSIONS

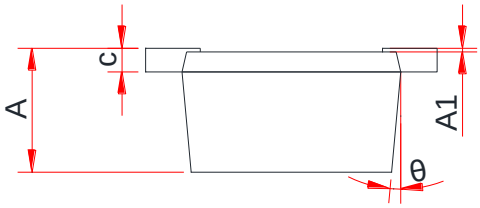
SOT-563



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.45	0.52	0.60
A1	0.00	—	0.05
e	0.50BSC		
c	0.09	—	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.10	—	1.45
b	0.17	0.22	0.27
L	0.15Ref		
L1	0.25Ref		
θ	7° Ref		

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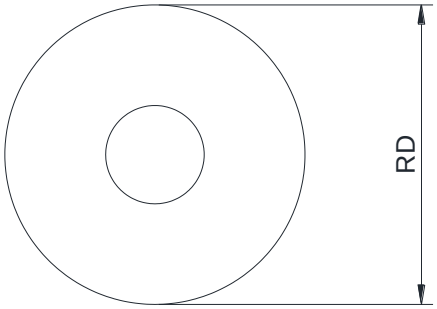
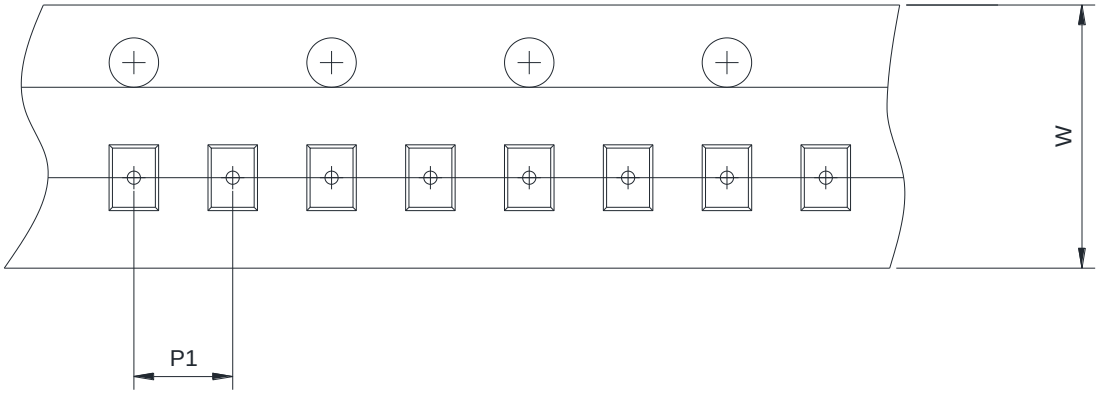
TAPE AND REEL INFORMATION

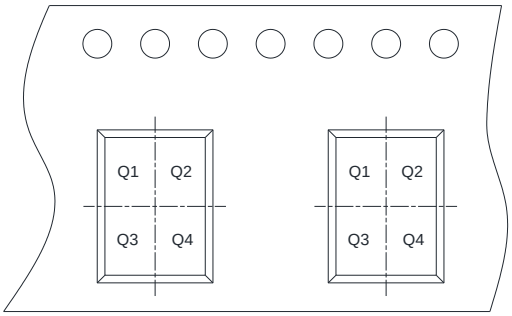
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



User Direction of Feed

RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☐ Q1	☐ Q2	☑ Q3	☐ Q4

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