Thermal Overload Protection

The WD1050C08 has a thermal overload protection function that operates to protect itself from short-term misuse and overload conditions. When the junction temperature exceeds around 155°C, the device inhibits operation. Both the PFET and the NFET are turned off. When the temperature drops below 125°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

Soft Start

The WD1050C08 has a soft-start circuit that limits in-rush current during startup. During startup the switch current limit is increased in steps. Soft start is activated if EN goes from low to high after V_{IN} reaches 2.7V.

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Application Informations

Output Voltage Setting

The WD1050C08 features a pin-controlled adjustable output voltage to eliminate the need for external feedback resistors. It can be programmed for an output voltage from 0.6V to 3.4V by setting the voltage on the VCON pin, as in the following formula:

$$V_{OUT} = 2.5 \times VCON \quad (1)$$

When VCON is between 0.24V and 1.36V, the output voltage will follow proportionally by 2.5 times of VCON.

If VCON is less than 0.24V (V_{OUT} = 0.6V), the output voltage may be regulated. Refer to datasheet curve (Low VCON Voltage vs. Output Voltage) for details. This curve exhibits the characteristics of a typical part, and the performance cannot be guaranteed as there could be a part-to-part variation for output voltages less than 0.6V.

Inductor Selection

There are two main considerations when choosing an inductor: the inductor should not saturate, and the inductor current ripple should be small enough to achieve the desired output voltage ripple. Different manufacturers follow different saturation current rating specifications, so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings over the ambient temperature of application should be requested from manufacturer.

Minimum value of inductance to guarantee good performance is 0.3 µH at bias current (ILIM (typ.)) over the ambient temperature range. Shielded inductors radiate less noise and should be preferred. There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current should be greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as:

$$I_{SAT} > I_{OUT\_MAX} + I_{RIPPLE}$$

Where

$$I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 \times L}\right) \times \left(\frac{V_{OUT}}{V_{IN}}\right) \times \left(\frac{1}{f}\right)$$

- I_{RIPPLE}: average-to-peak inductor current
- I_{OUT_MAX}: maximum load current (750 mA)
- V_{IN}: maximum input voltage in application
- L: minimum inductor value including worst-case tolerances (30% drop can be considered for Method 1)
- F: minimum switching frequency (5 MHz)
- V_{OUT}: output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that can handle the maximum current limit of 1600 mA.

The inductor's resistance should be less than around 0.1Ω for good efficiency.

Capacitor Selection

The WD1050C08 is designed for use with ceramic capacitors for its input and output filters. Use a 10 µF ceramic capacitor for input and a 4.7 µF ceramic capacitor for output. They should maintain at least 50% capacitance at DC bias and temperature conditions. Ceramic capacitors type such as X5R, X7R, and B are recommended for both filters. They provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. DC bias characteristics of the capacitors must be considered when selecting the voltage rating and case size of the capacitor. For CIN, use of an 0805 (2012) size may also be considered if there is room on the system board.

The input filter capacitor supplies AC current drawn by the PFET switch of the WD1050C08 in

the first part of each cycle and reduces the voltage ripple imposed on the input power source. The output filter capacitor absorbs the AC inductor current, helps maintain a steady output voltage during transient load changes, and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR (Equivalent Series Resistance) to perform these functions. The ESR of the filter capacitors is generally a major factor in voltage ripple.

PC Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the CSP-6L package and board pads — poor solder joints can result in erratic or degraded performance. Good layout for the WD1050C08 can be implemented by following a few simple design rules, as illustrated in below Figure.

1. Place the WD1050C08, inductor, and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching current and act as antennae. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the VIN and GND pads.
2. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor, through the WD1050C08 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the WD1050C08 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. Connect the ground pads of the WD1050C08 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the WD1050C08 by giving it a low impedance ground connection.
4. Use side traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
5. Route noise sensitive traces such as the voltage feedback path away from noisy traces between the power components. The output voltage feedback point should be taken approximately 1.5 nH away from the output capacitor. The feedback trace also should be routed opposite to noise components. The voltage feedback trace must remain close to the WD1050C08 circuit and should be routed directly from FB to VOUT at the inductor and should be routed opposite to noise components. This allows fast feedback and reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.

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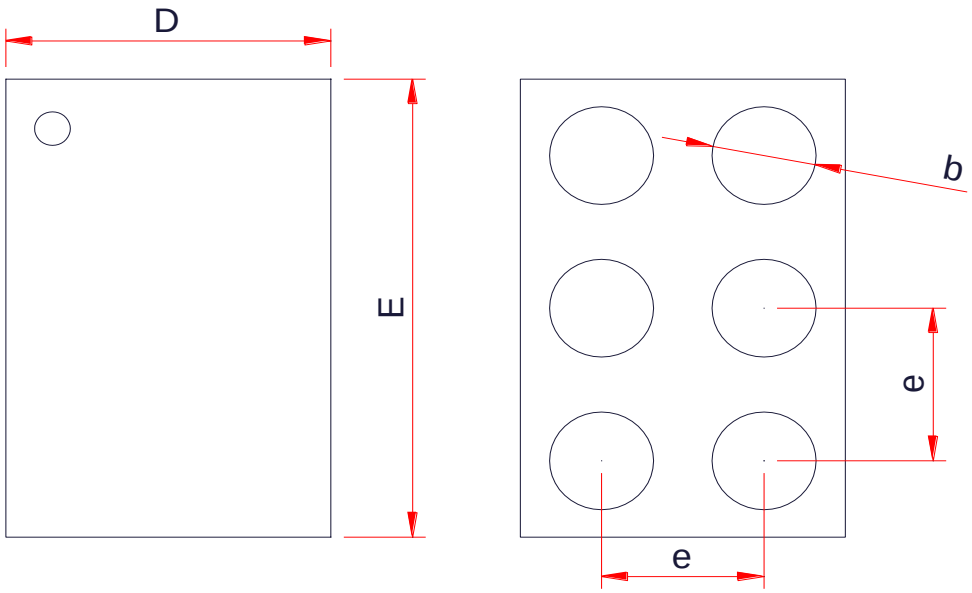
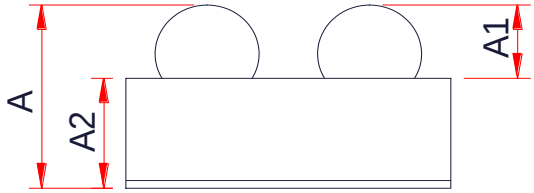
PACKAGE OUTLINE DIMENSIONS

CSP-6L



TOP VIEW

BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.53	0.57	0.60
A1	0.16	0.19	0.21
A2	0.36	0.38	0.40
D	0.94	0.97	1.00
E	1.44	1.47	1.50
e	0.50 Typ.		
b	0.21	0.23	0.25

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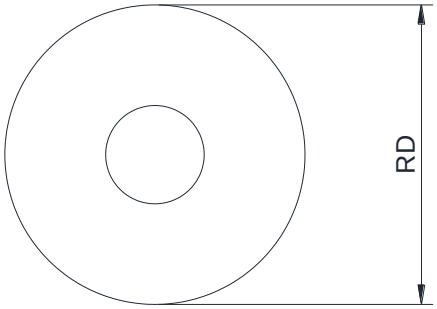
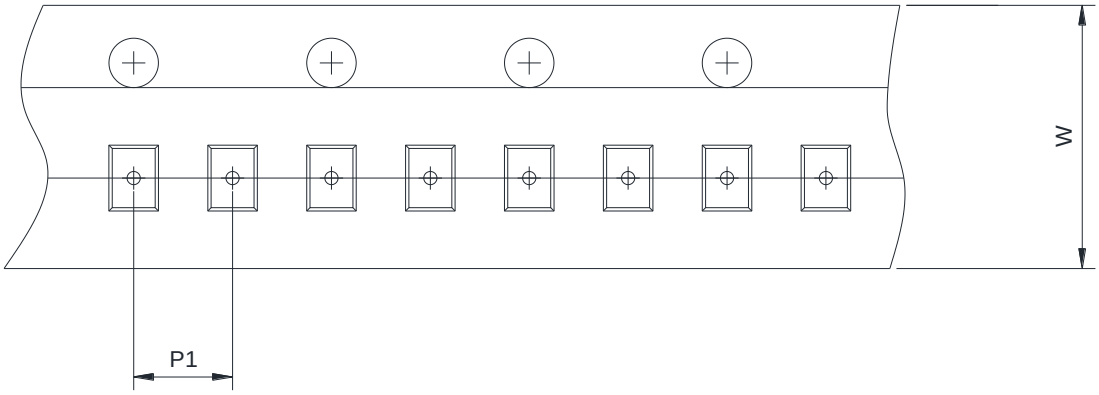
TAPE AND REEL INFORMATION

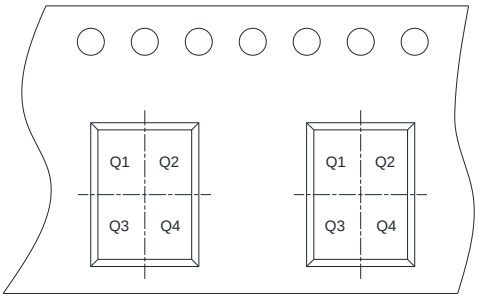
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



User Direction of Feed

RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4

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