Typical Applications

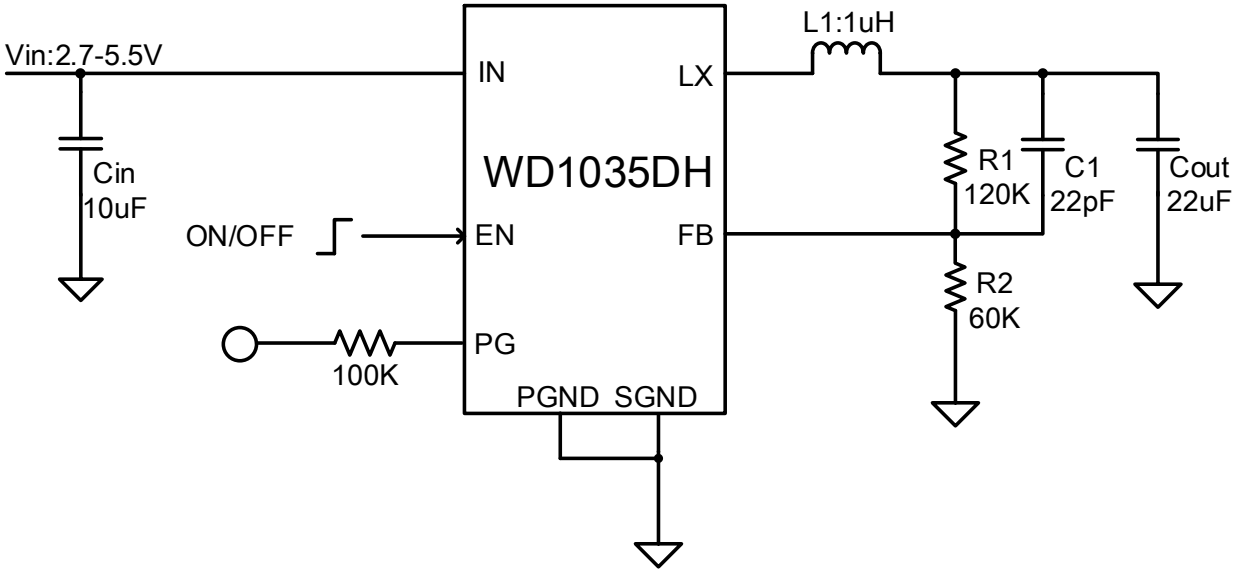


Fig1 Schematic Diagram

Pin Descriptions

Pin Name	Pin Number	Pin Description
FB	1	Feedback pin. Connected to the feedback resistor for adjustable version or VOUT for fix output version.
PG	2	Power good indicator. The output of this pin is an open-drain with external pull-up resistor. PG is pulled up when the FB voltage is within 90%, otherwise it is LOW.
IN	3	Input pin. Decouple this pin to GND with at least 10uF ceramic Cap.
PGND	4	Power Ground.
NC	5	No Internal Connection.
LX	6	Inductor pin.
EN	7	Enable Control. Pull high to turn on. Do not leave it floating .
SGND	8	Signal Ground.
Exposed Pad		The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.

4275 Burton Drive
Santa Clara, CA 95054
USA

Tel: + 1 408 567 3000
Fax: + 1 408 567 3001
www.ovt.com

Absolute Maximum Ratings (1)

Parameter		MIN	MAX	Unit
Power Supply VCC		-0.3	6.5	V
Others Pins		-0.3	VCC+0.6	V
Power Dissipation, P_D @ T_A=25℃， DFN2X2-8L			2.19	W
Package Thermal Resistance T_{JA}			50	°C /W
Package Thermal Resistance T_{JC}			8	°C /W
Junction Temperature T_J			150	°C
Lead Temperature (Soldering,10 sec)			260	°C
Storage Temperature Range		-65	150	°C
ESD Ratings	HBM	2000		V
	CDM	2000		V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	MIN	MAX	Unit
Power Supply VCC	2.7	5.5	V
Junction temperature T_J	-40	125	°C
Ambient temperature T_A	-40	85	°C

4275 Burton Drive
Santa Clara, CA 95054
USA

Tel: + 1 408 567 3000
Fax: + 1 408 567 3001
www.ovt.com

Electronics Characteristics

Unless otherwise specified: limits for typical values are for T_A = 25℃ and minimum and maximum limits apply over the operating ambient temperature range (-40℃ < T_A < 85℃); VIN=4.2V,Vout=2.5V,L1=1uH,Cout=22uF.

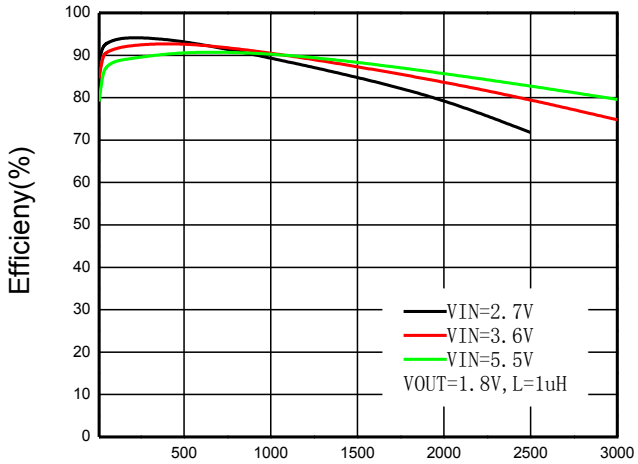
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Voltage Range	V_{IN}		2.7		5.5	V
VIN Under Voltage Lockout	V_{UVLO}-H	V_{IN} Rising		2.45		V
	V_{UVLO}-L	V_{IN} Falling		2.25		V
Quiescent Current	I_Q	Switching		45		uA
Shutdown Current	I_{SD}	V_{EN} =GND, V_{IN} =3.6V			1	μA
Feedback Reference	V_{REF}		0.588	0.6	0.612	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$			0.35		%/V
PFET Rdson	Rdson P			100		mΩ
NFET Rdson	Rdson N			60		
PFET Current Limit	ILIMT			4.5		A
Oscillator Frequency	F_{OSC}			1.5		MHz
Max Duty Cycle				100		%
Soft Start Time				800		uS
Power on delay time				25		uS
Input OVP shutdown	V_{OVP}	Rising		6.3		V
		Falling	5.6	6		V
Over Volatage Protection Blanking Time				20		uS
Thermal Shutdown				150		°C
Thermal Shutdown Hysteresis				30		°C
EN Input LOW Voltage	V_{IL}				0.4	V
EN Input HIGH Voltage	V_{IH}		1.4			V

4275 Burton Drive
Santa Clara, CA 95054
USA

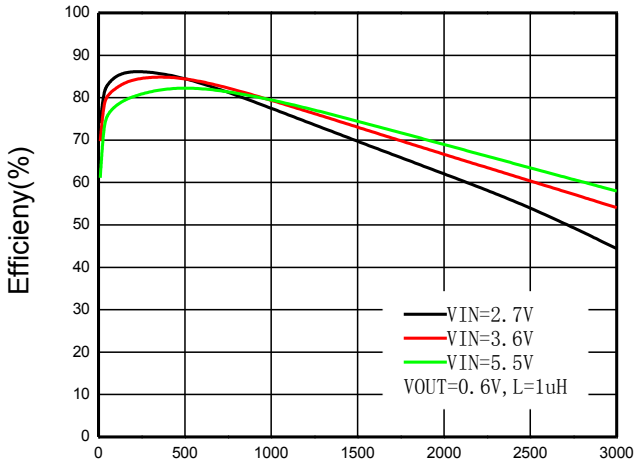
Tel: + 1 408 567 3000
Fax: + 1 408 567 3001
www.ovt.com

Typical Characteristics

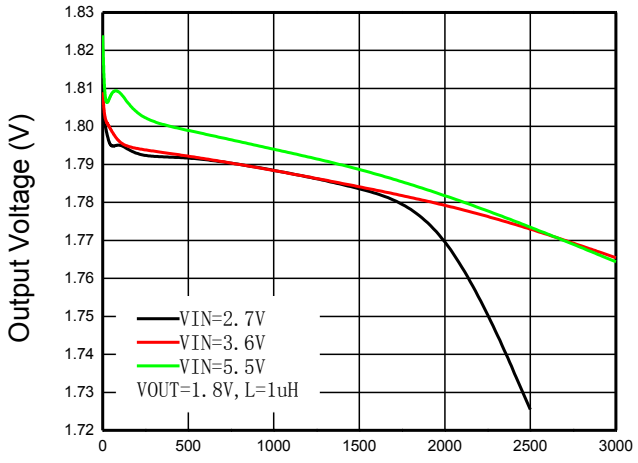
(Ta=25°C, V_{IN}=5V, V_{EN}=V_{IN}, C_{IN}=10μF ,C_{OUT}=22μF, L1=1μH, unless otherwise noted)



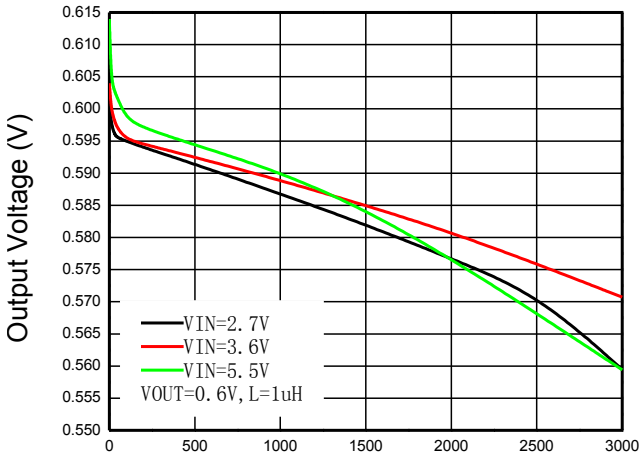
Efficieny vs.Load Current



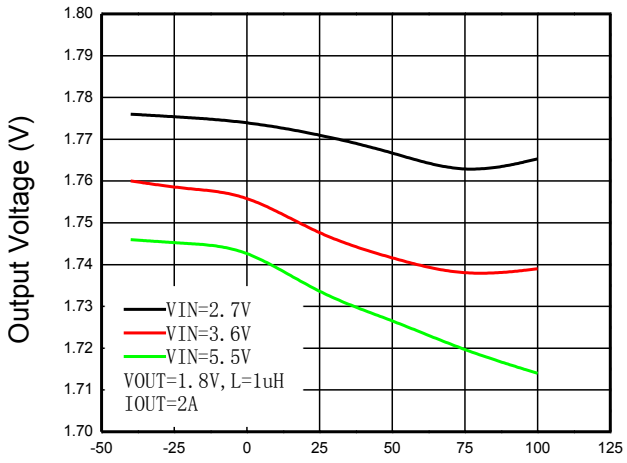
Efficieny vs.Load Current



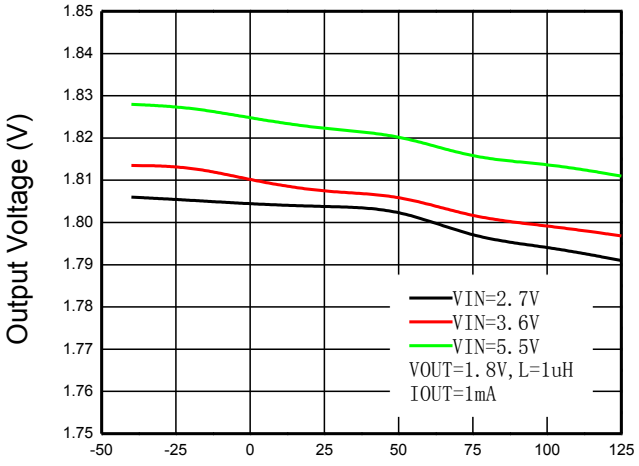
Output Voltage vs.Output Current



Output Voltage vs.Output Current



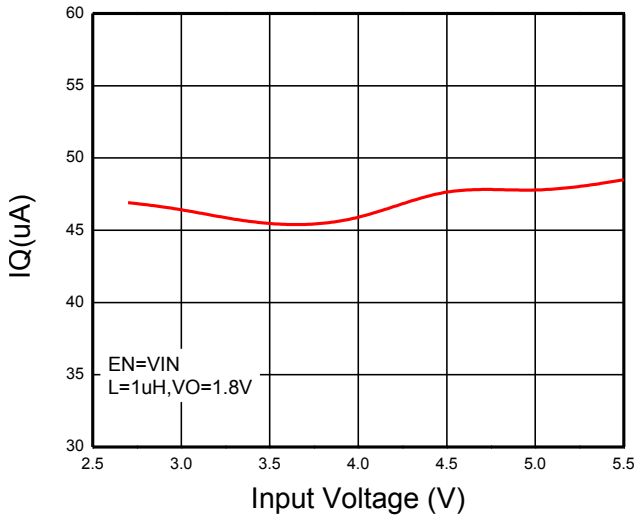
Output Voltage vs.Temperature



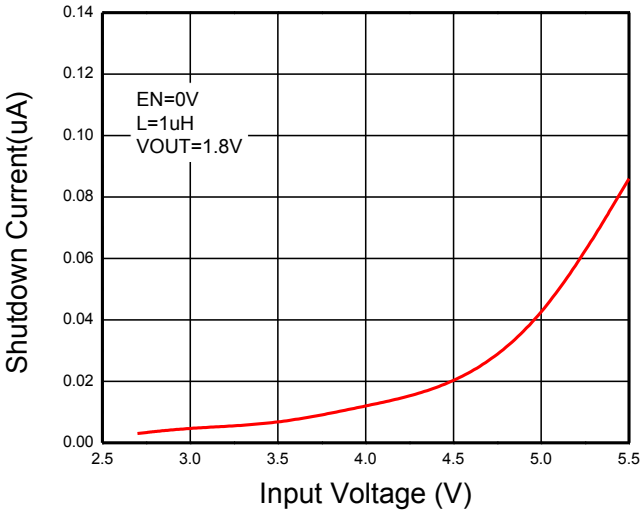
Output Voltage vs.Temperature

4275 Burton Drive
Santa Clara, CA 95054
USA

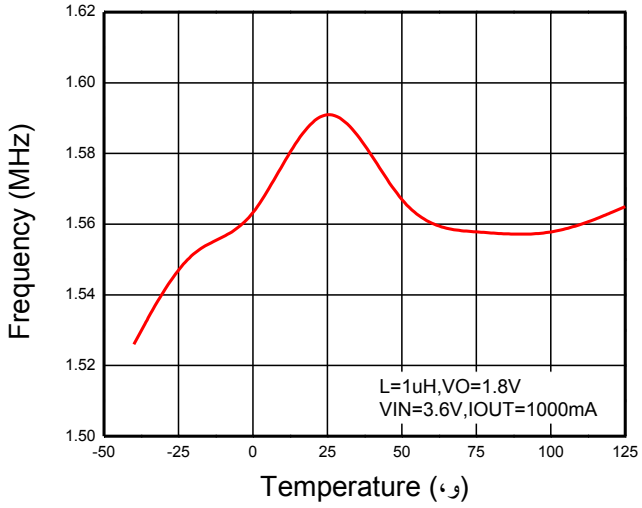
Tel: + 1 408 567 3000
Fax: + 1 408 567 3001
www.ovt.com



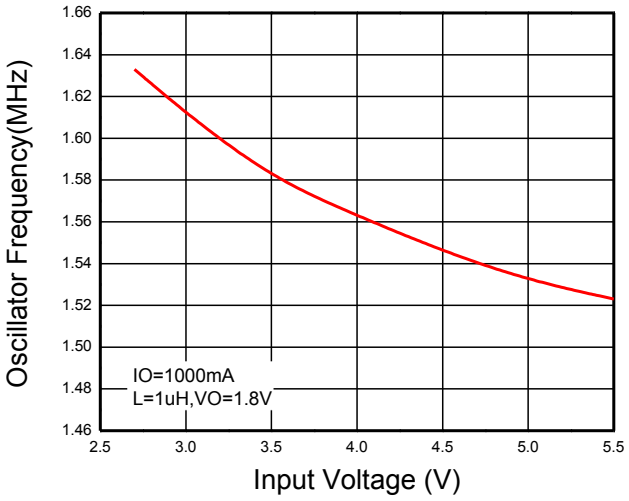
Supply Current vs. Input Voltage



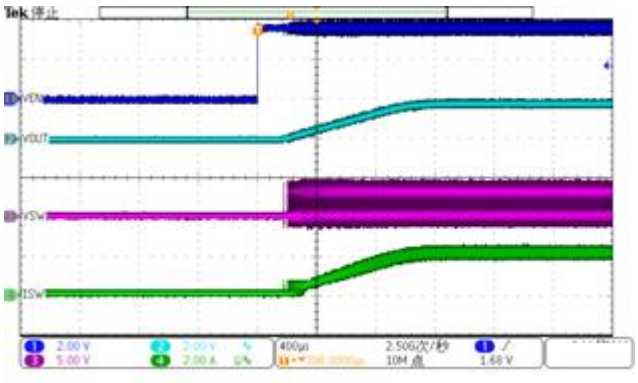
Shutdown Current vs. Input Voltage



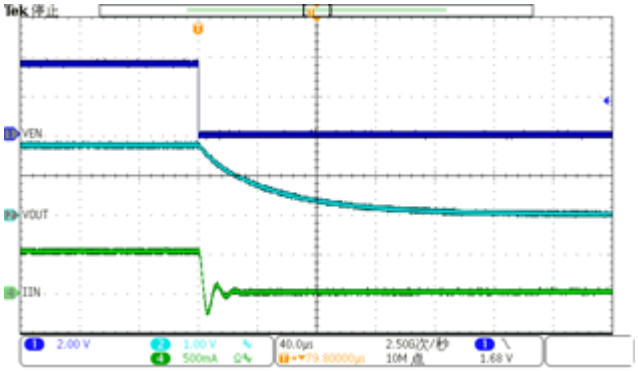
Frequency vs. Temperature



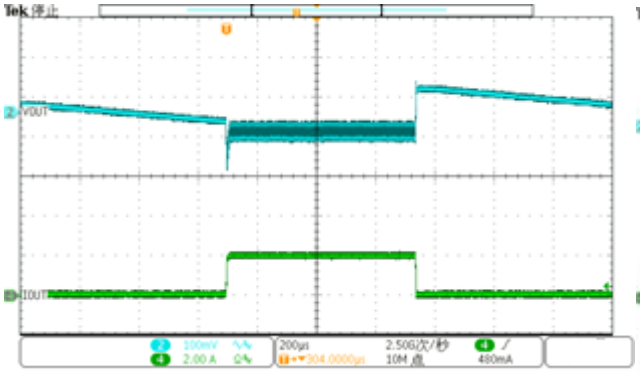
Oscillator Frequency VS. Input Voltage



VIN=3.6V, VO=1.8V，EN=3.6V , IO=2A, EN On

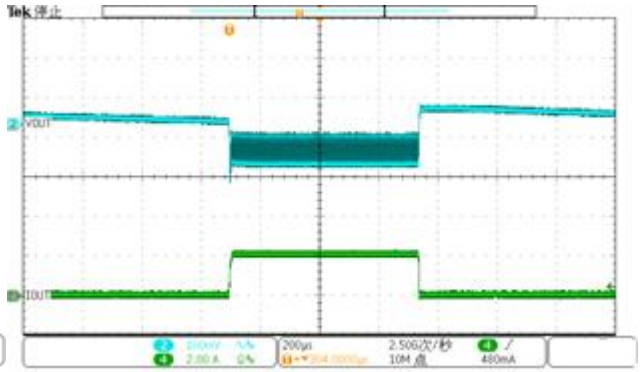


VIN=3.6V, VO=1.8V，EN=3.6V , IO=1A, EN Off



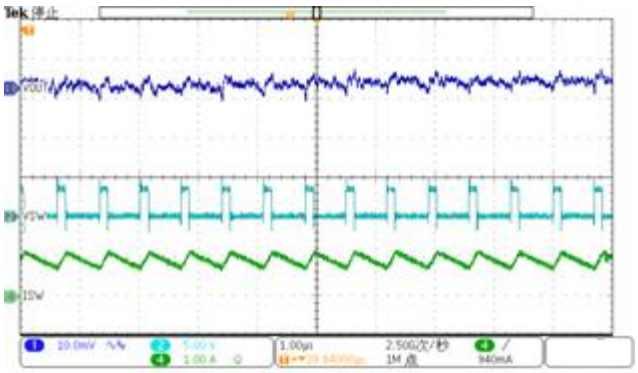
Load Transient Response

VIN=5V,VO=1.8V,EN=3.6V,IO=1mA-2A

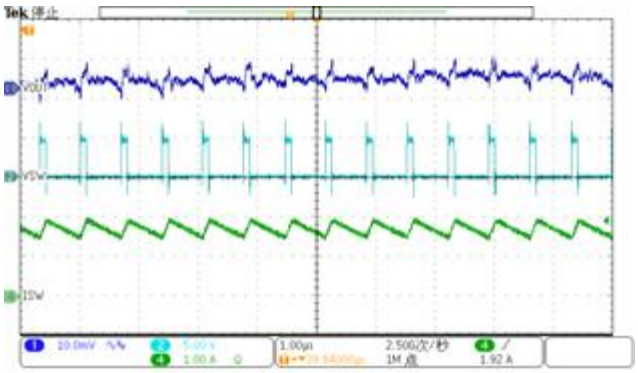


Load Transient Response

VIN=5V,VO=0.6V,EN=5V,IO=1mA-2A



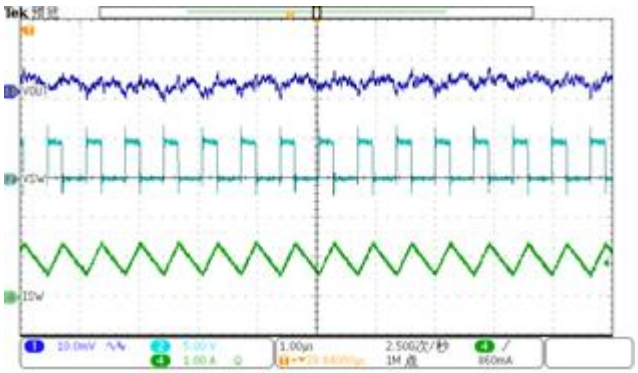
Ripple : VIN=5.0V, VO=0.6V，EN=3.6V　IO=1A



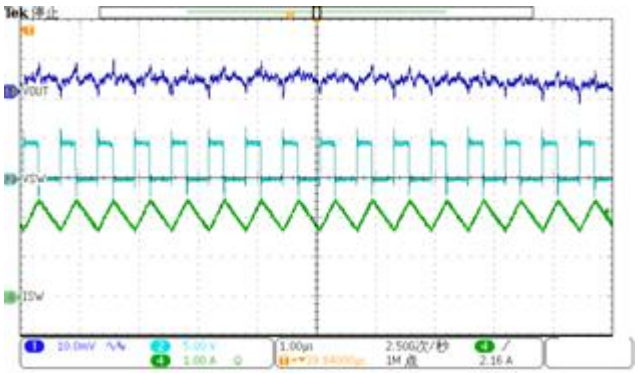
Ripple : VIN=5.0V, VO=0.6V，EN=3.6V　IO=2A

4275 Burton Drive
Santa Clara, CA 95054
USA

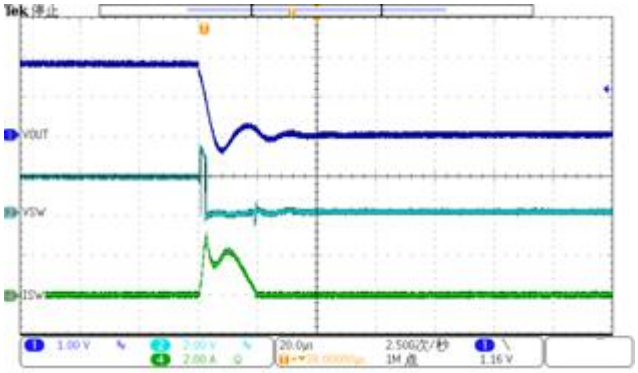
Tel: + 1 408 567 3000
Fax: + 1 408 567 3001
www.ovt.com



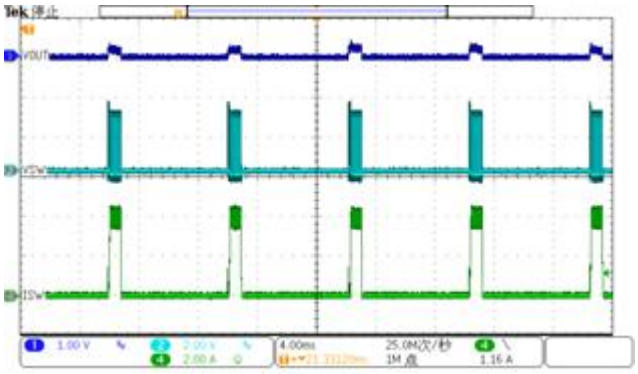
Ripple : VIN=5.0V, VO=1.8V，EN=3.6V　IO=1A



Ripple : VIN=5.0V, VO=1.8V，EN=3.6V　IO=2A



VIN=3.6V, VO=1.8V，EN=3.6V　VOUT short



Operation Information

WD1035DH is a high efficiency 1.5MHz synchronous Step-Down DC/DC regulator IC capable of delivering up to 3A output current. It can operate over a wide input voltage range from 2.7V to 5.5V and integrate main switch and synchronous switch with very low R_{DSON} to minimize the conduction loss.

Application Information

Because of the high integration in the WD1035DH IC, the application circuit based on this regulator IC is rather simple. Only input capacitor Cin, output capacitor Cout, output inductor L and feedback resistors (R_H and R_L) need to be selected for the targeted applications specifications.

Feedback resistor dividers R_H and R_L :

Choose RH and RL to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose larger resistance values for both R_H and R_L. A value of between 100kΩ and 1MΩ is highly recommended for both resistors. If R_L =120kΩ is chosen, then R_H can be calculated to be:

$$R_H = \frac{(V_{out} - 0.6V) * R_L}{0.6V}$$

Input capacitor C_{IN} :

A Typical X7R or better grade ceramic capacitor with 10V rating and greater than 10uF capacitor is recommended. To minimize the potential noise problem, place this ceramic capacitor really close to the VIN and GND pins. Care should be taken to minimize the loop area formed by C_{IN} ,and VIN/GND pins.

Output inductor L :

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{out}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX\times 40\%}}$$

Where Fsw is the switching frequency and Iout,max is the maximum load current.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{out}/V_{IN,MAX})}{2 * F_{SW} * L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<25mΩ to achieve a good overall efficiency.

Inductor vs. Output Capacitor:

The ripple base control strategy need very little COUT to confirm stability. Too large inductor and COUT will lead to instability.

Power good:

The WD1035DH has a power good output. The PG pin goes high impedance once the output is above 90% and below 110% of the nominal voltage, and is driven low once the output voltage falls below typically 85% or above 115% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

OCP and SCP protection :

With load current increasing, the NFET current will get higher than valley current limit threshold. The

NFET will keep turning on until NFET current decrease to the valley current limit threshold, so that valley current is limited. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 30% of the regulation level, output short is detected and the IC will work in hiccup mode. During the hiccup, the regulator waits every 8 soft-start time before a soft-start. If at the time of soft-start finish, VOUT is still below 30% of the regulation level, the regulator will wait another 8 soft-start time before another soft-start. The hiccup reduces the power dissipation of the IC under short circuit conditions. If the hard short is removed, IC will go back to normal operation.

Layout Consideration

The layout design of WD1035DH regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: Cin, L, R_H and R_L.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) Cin must be close to Pins VIN and GND. The loop area formed by Cin and GND must be minimized. Cout must be close to the Chip, too.

3) The PCB copper area associated with SW pin must be minimized to avoid the potential noise problem.

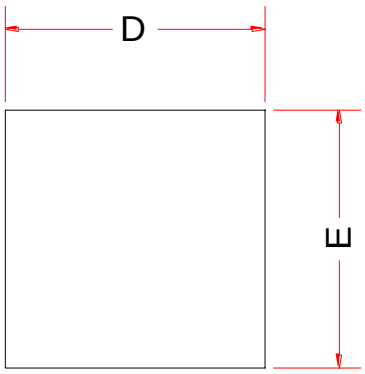
4) The components R_H and R_L, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem.

4275 Burton Drive
Santa Clara, CA 95054
USA

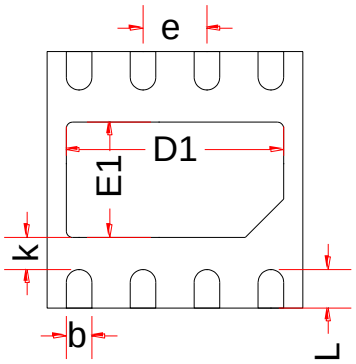
Tel: + 1 408 567 3000
Fax: + 1 408 567 3001
www.ovt.com

PACKAGE OUTLINE DIMENSIONS

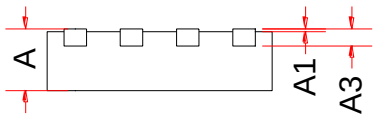
DFN2x2-8L



TOP VIEW



BOTTOM VIEW



SIDE VIEW

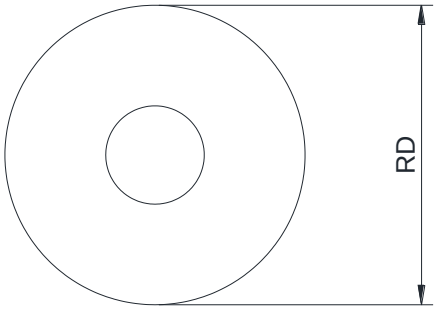
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.00		0.05
A3	0.15Ref		
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D1	1.60	1.70	1.80
E1	0.80	0.90	1.00
k	0.20	-	-
b	0.15	0.20	0.25
e	0.50BSC		
L	0.25	0.30	0.35

4275 Burton Drive
Santa Clara, CA 95054
USA

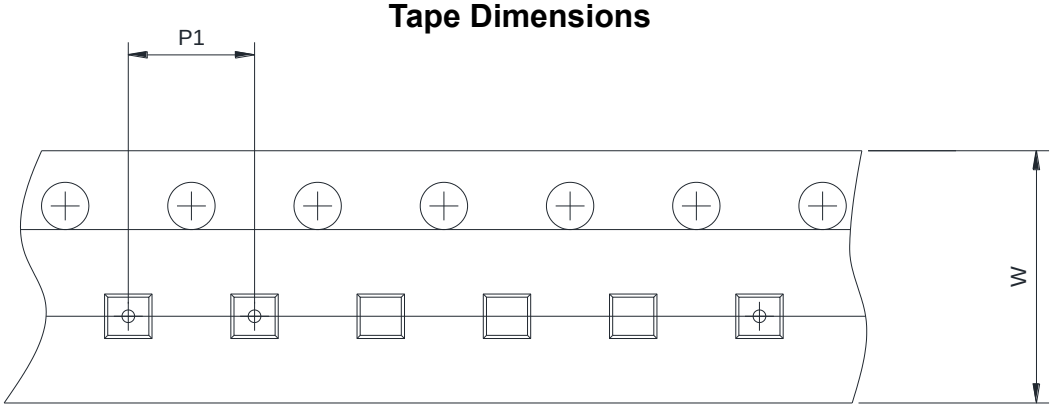
Tel: + 1 408 567 3000
Fax: + 1 408 567 3001
www.ovt.com

TAPE AND REEL INFORMATION

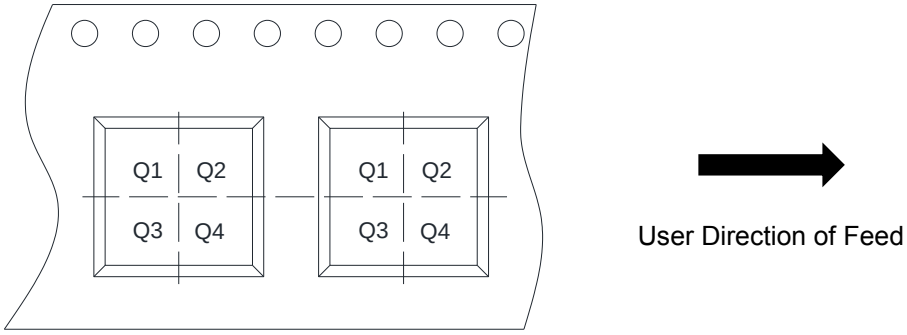
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☑ Q1	☐ Q2	☐ Q3	☐ Q4

4275 Burton Drive
Santa Clara, CA 95054
USA

Tel: + 1 408 567 3000
Fax: + 1 408 567 3001
www.ovt.com